Design and Simulation of SIGMA DELTA ADC

A thesis submitted in partial fulfillment

of the requirements for the degree of

Master of Technology

in Electronics and Communication Engineering

By

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Under the guidance of

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To my parents

Department of Electronics and Communication Engineering
National Institute of Technology
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CERTIFICATE

This is to certify that the work done for the direction of thesis entitled**" Design and simulation of 1-bit SIGMA DELTA ADC using CADENCE Tool"** submitted by ***Ms. SoumyaSuravita Guru*** (**211EC2080**) in partial fulfillment of the requirements for the award of Master of Technology Degree in Electronics and Communication Engineering with specialization in VLSI Design and Embedded Systems at National Institute of Technology, Rourkela is an authentic work carried out by her under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University/Institute for the award of any Degree or Diploma.

Place: NIT Rourkela
Date: 24th May, 2013

Dr. Debiprasad Priyabrata Acharya
Associate Professor

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Soumya Suravita Guru

ABSTRACT

Analog-to-digital converters play an essential role in modern RF receiver design.Conventional Nyquist converters require analog components that are precise andHighly immune to noise and interference. In contrast, oversampling converters can be implemented using simple and high-tolerance analog components. Moreover,Sampling at high frequency eliminates the need for abrupt cutoffs in the analog antialiasing filters. A technique of noise shaping is used in Σ-Δ converters in addition to oversampling to achieve a high-resolution conversion. A significant advantage of the method is that analog signals are converted using simple and high-tolerance analog circuits, usually a 1-bit comparator, and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter.

In this paper, the design technique for a low-cost first order narrow band sigma-delta modulator in a standard 0.9*μm CMOS* technology is described .This circuitry performs the function of an analog-to-digital converter. A first-order 1-bit sigma-delta (Σ-Δ) analog-to-digital converter is designed and simulated using Cadence 0.9μm CMOS process technology with power supply of 1.8 V through Cadence. The analysis of sigma-delta modulator structures and the design flow were given. The modulator is proved to be robustness, the high performance in stability .The simulation are compared with those from a traditional analog-to-digital converter to prove that sigma-delta is performing better in the case of weak signals acquisition. The design flow consist of a op-amp one of the key component of sigma delta adc which is used for designing of integrator and summing circuit , followed by a high speed comparator and a digital -to-analog convertor in the feedback path.

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1. INTRODUCTION

INTRODUCTION

1.1 MOTIVATION

Recent research on Radio Frequency (RF) communication emphasizes both higher integration, to meet customer demand for low-cost, low-power, small-form factor personal communication device .This reduction in power can be achieved by moving towards smaller feature size .However, as we move towards smaller feature size, the process variations and other non-idealities will greatly affect the performance of the device. One of theapplications where low power dissipation, low noise, high speed, less Offset voltage are required is Analog to Digital Converters (ADC) for mobile and portable devices. The performance limiting factor of such ADC is gain amplifiers and comparators. In wireless application oversampling analog-to-digital conversion has become popular because of its increased performance and flexibility. Oversampling uses a sampling rate that is much greater than the bandwidth of the signal of interest. Digital signal processing is then further used for filtering and down sampling. Sigma-delta ADC is a low-cost, low-bandwidth, low-power, high-resolution ADC and has varied applications in data acquisition, communications, signal processing and instrumentation. It had its origins in the early development phases of pulse code modulation (PCM) systems, this technique has been in existence for many years, but recent advance in technology has made this device practical and there use is becoming widespread, it has become a choice for modern voice band, audio and high resolution industrial measurement application. The Sigma Delta ADC is now used for much low cost, low power, high resolution applications.

1.2 THESIS GOALS

The main objective of this thesis is to design a Sigma Delta ADC using 90um Cadence technology. This describes the designing of different blocks needed for designing the modulator and filter architecture of the ADC.

1.3 THESIS ORGANIZATION

This thesis provides the designing of a Sigma Delta ADC using 90um cadence technology. The thesis can be organized in the following manner.

Chapter2 focuses on Basics of Analog-To-Digital Converter (ADC), Different architectures of ADCs are studied in this section along with advantages and disadvantages. It gives a detail over view of Sigma Delta ADC architecture and functionality.

Chapter 3 Describes the Designing detail of Sigma Delta ADC,it gives a brief description about the different components of the ADC and also describes it designing requirements of these components.

Chapter4 Gives the Transistor level designing of the ADC. It describes the detail designing of Sigma Delta ADC using 90um CMOS technology, it includes he designing of different parts of the modulator and the decimator part. All the simulated result using cadence tool of different blocks of the modulator is shown in this chapter including the final ADC architecture and its result.

2. Sigma Delta Overview

2.1 Analog-to-digital conversion:

Data converter is a key component in any electronic system. Real world signals are inherently analog; however, the digital form of analog signals can be processed using robust, flexible and reliable digital-signal-processing (DSP). Therefore, analog-to-digital conversion becomes critical. Data converter is also a very critical component in wireless receivers. Different radio-frequency (RF) receiver architectures have different specifications on their analog-to-digital-converters (ADCs). Sigma-Delta modulation based analog-to digital (A/D) conversion process is a cost effective and an alternative for high resolution converters which can be ultimately integrated on digital signal processor ICs. The sigma-delta modulator was first introduced in early phase of pulse width modulation (PWM) in around 1962; but it gained its importance in recent times after the development in digital VLSI technologies.

Conventional converters are often difficult to implement in (VLSI) technology. As these conventional methods need precise analog components in their filters and conversion circuits and their circuits are very vulnerable to noise and interference. The conventional methods uses low sampling frequency, which is usually the nyquist rate of the signal. By keeping these things in mind the people are going for over sampling converters, these converters make extensive use of digital signal processing. The main advantages of the sigma delta □A/D converters are mentioned below.

1. Higher reliability.
2. Increased functionality.
3. Reduced chip cost.

The Sigma Delta ADC are now used for many low cost, low power, high resolution applications, the key feature of this ADC is that it is based on oversampling method which uses high

frequencies modulation technique and eliminates the use of anti aliasing filter at the input to the converter.

2.2 SIGMA-DELTA ADC

Depending upon the sampling rate Analog-to-Digital Converter (ADC) can be divided in to two parts. One which samples the signal at Nyquist rate that is fN=2F, Where fN is the sampling rate and F is the bandwidth of the input signal, while the other samples the signal at a much higher sampling rate then the signal band width this type of sampling is called oversampling and the converters are called oversampling converters. These converters have an ability to achieve high resolution, high reliability, and performance. Then Nyquist rate converters, some of the Nyquist rate converters are

- Flash ADC
- Digital Ramp ADC
- Successive Approximation ADC
- Tracking ADC
- Pipeline ADC

2.3Flash ADC

Flash ADC's are also called parallel ADCs. Due to the parallel architecture it is the fastest ADC among all the other types and are suitable for high bandwidth applications. Due to presence of 2 N resistor it consumes a lot of power, has low resolution, and expensive for high resolution. Itis mainly used in high frequency applications and in the other types of ADC architectures

e.g.multi bit sigma delta and pipelined. Few applications of flash ADCs are satellite communication,radar processing, data acquisition, sampling oscilloscopes, and high-density disk drives. A typicalflash ADC block diagram is shown in Figure **2.1**

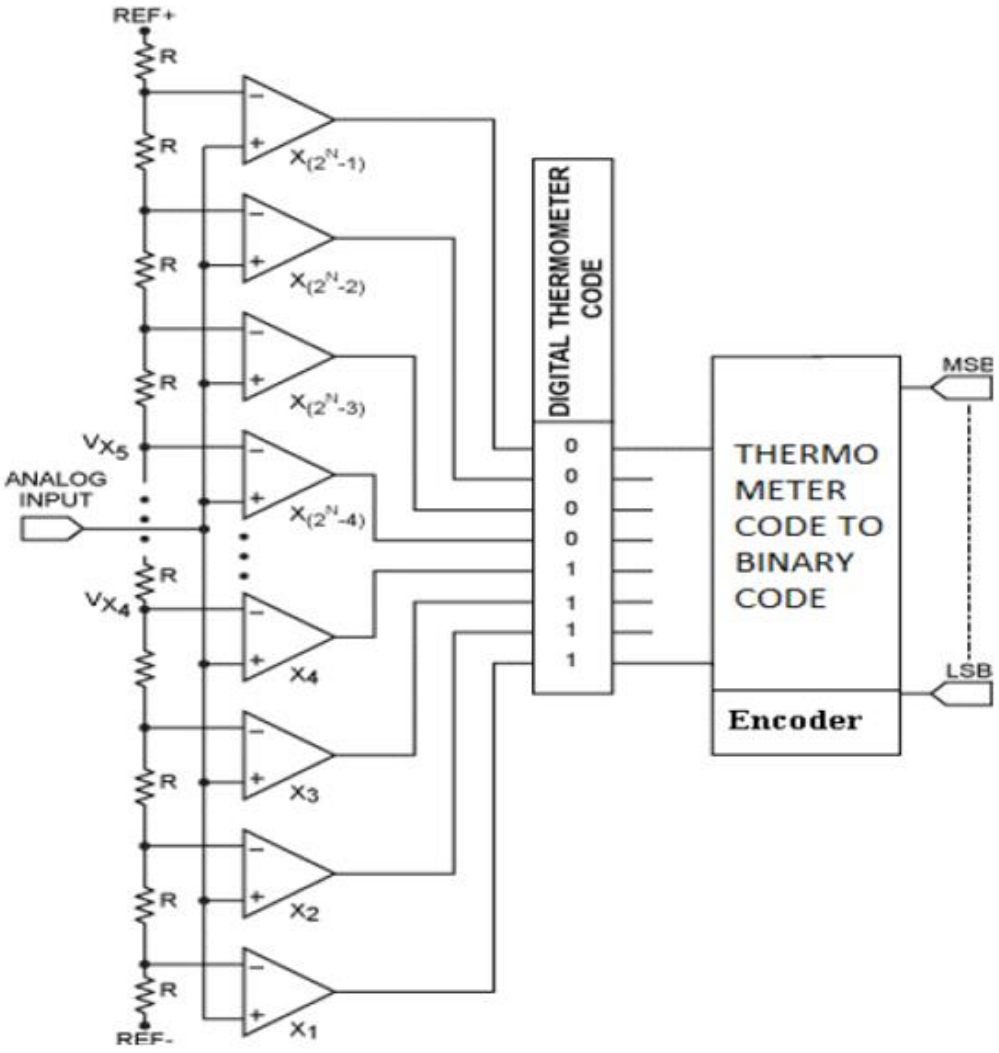


Figure 2.1 Architecture of Flash ADC

Here 2N – 1 comparators are required for an "N" bit converter. The resistor ladder network is formed by 2N resistors, which is used to generatethe reference voltages for the each comparator. The reference voltage for each comparator is 1 leastsignificant bit (LSB) less than the reference voltage for the comparator immediately above it. When the input voltage (positive terminal) is

higher than the reference voltage (negative voltage) of comparator it will generate a "1", otherwise, the comparator output is "0". If the analog input isin between Vx4 and Vx5 , then the comparators X1 through X4 generates "1"s and all the remainingcomparators generate "0"s.

The comparators will generate a thermometer code of an input signal. It is called thermometer code encoding, because it is similar as mercury thermometer, where in the mercury column, the mercury always rises to the appropriate temperature and no mercury is present above that temperature. This thermometer code will then encode into a binary form by thermometer-to binary encoder. “The comparators are typically a latched comparator with low gain stages. They are typically low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. They are designed to obtain the low voltage offset, such that the condition of the comparator is that its input offset of each comparator is smaller than 1 LSB of the ADC. Otherwise, the offset of the comparator could falsely trip the comparator, resulting in a digital output code not representative of a thermometer code. A regenerative latch present at each comparator output stores the result. Due to presence of positive feedback, the end state is forced to either a "1" or a “0”.

2.4Pipelined ADC

The pipelined analog-to-digital converter is one of the most popular ADC architecture. It can work from few Msamples to more than hundreds of Msamples with resolution from 8 bit to 16bits. Due to its high resolution and sampling rate range it is widely use in medical and communication applications e.g. CCD imaging, digital receiver, ultrasonic medical imaging, base station, digital video (for example, HDTV), DSL, cable modem, and fast Ethernet. Speed, resolution, power and dynamic performance are greatly improved in Pipeline ADC but SAR and

Integrating architectures are still used for low sampling rate applications, whereas for high sampling rate (e.g. 1 GHz) flash ADC is still the choice. The example of 12 bits pipeline ADC isshown inFigure **2.2**

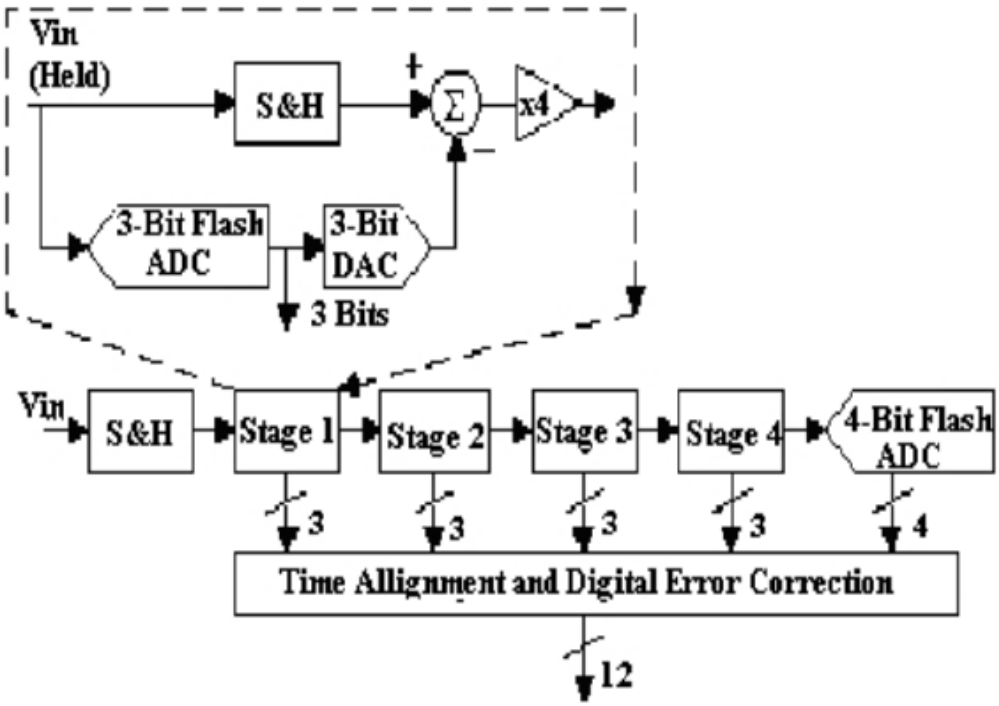


Figure 2.2 Architecture of Pipe Line ADC

Initially sample-and-hold (S&H) circuit samples and holds the input V_{IN}. The flash ADC in the first stage will convert this signal into 3 bit digital output. This 3 bits digital code is applied to DAC and the analog output is subtracted from the original signal, then the remainder is multiplied by 4 and then applied to the next stage. This process will continue till the last stage (Stage 4) and every stage provides 3 bits. After last stage the amplified remainder signal is feedinto 4 Bit flash ADC that will generate 4 least significant bits. As every stage generates bits at different instant in time therefore it is required to align all the bits by shift register prior to applying 12-bit digital output to the digital-error-correction logic. During the interval when one

stage completes the processing of one sample and passes the magnified remainder to the other stage. The next stages are also performing the same operation because sample and hold circuit is Embedded in every stage. This pipelining technique explained above increases the throughput of ADC.

2.5Successive Approximation ADC

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are mostly use in medium to high-resolution and low sampling rate applications. These are mostly in the rangebetween 8 to 16 bits. It also provides small form factor and low power consumption. As its power consumption is low therefore it is the good choice for low power application such as Portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition. SAR ADC actually implements binary search algorithm, therefore its internal circuitry might work at several megahertz but due to the successive approximation algorithm the sampling rate of ADC is quite small. There are many ways to implement SAR ADC but its basic structure is shown in Figure **2.3**

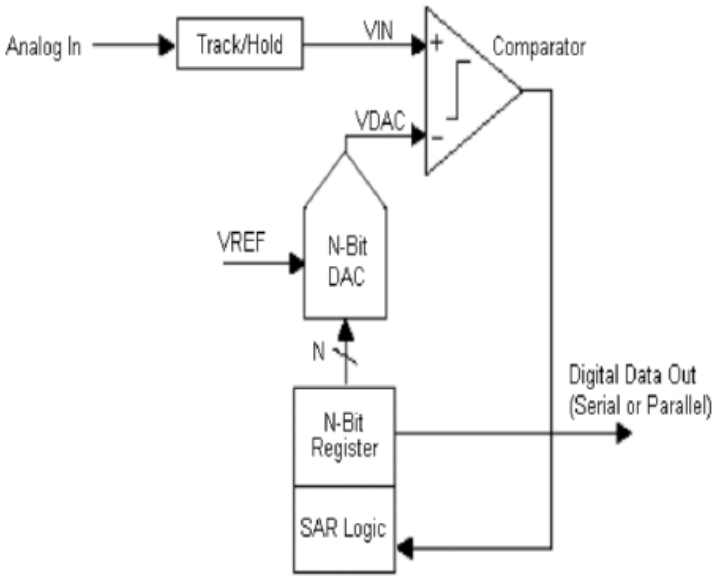
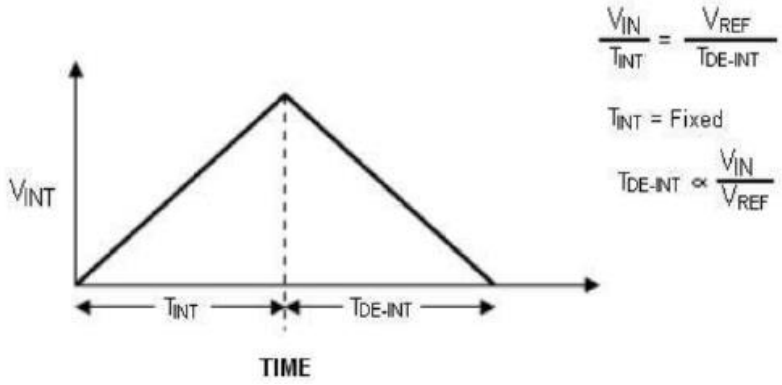


Figure 2.3 SuccessiveApproximation ADC

In this structure track/hold circuit is used to hold the analog input voltage (V_{IN}). The binarysearch algorithm is implemented by N-bits register. Initially the value of register is set to mid-scalier. MSB set to “1” and all the other bits are set to “0”. The output of DAC (V_{DAC}) becomes half the reference voltage $V_{REF}/2$, where V_{REF} is the reference voltage of ADC. The comparator will compare the input voltage V_{IN} with V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output will be set to “1”, and the MSB of the N-bit register remains at '1'. If the input voltage V_{IN} is less than V_{DAC} then the comparator output becomes “0”. The SAR control logic will change the MSB of the register to '0', set the next bit to “1” and perform comparison again. This process continues till LSB and once this process is completed the N-bit digital word is available in the register.

2.6Dual-Slope ADC

In order to understand the architecture of Dual slope ADC we first need to understand theconcept of single slope ADC. The single slope ADC is also known as integrating ADC and themain theme of this architecture is to use analog ramping circuit and digital counter instead of using DAC. The op-amp circuit that is also called an integrator is used to generate a reference ramp signal that will compare with input signal by a comparator. The digital counter clocked with precise frequency is used to measure time taken by the reference signal to exceed the input signal voltage. The Dual-Slope ADC input voltage (V_{IN}) integrates for fixed time interval (T_{INT}), then it will deintegrate by using reference voltage (REFV) for a variable amount of time ($T_{DE\text{-}INT}$) as shown in Fig.2.4



2.4 Dual Slope ADC

The behavior of this structure is similar to digital ramp ADC, except that saw-toothwaveform is used as reference signal. “Integrating ADCs provides high resolution and can provide good noise rejection and line frequency”. As dual slope structure integrates input signal for fixed time instant therefore input signal becomes average and this will produce output with greater noise immunity. Due to this fact it is very useful for high accuracy applications. The other advantage of this structure is that it avoids DAC in the structure that decreases the design complexity. The main limitation of this structure is that it only suitable for low bandwidth input signals.

2.7ADC comparison

It shows the range of resolutions, conversion method, encoding method, conversion time, size, advantages and disadvantages available for flash, sigma-delta, successive approximation, dual slope and pipeline converters. As one can observe that flash ADC provide the highest speed amongst all the other types of ADC. The speed of sigma delta converter is comparable with SAR ADC but even it is much slower than flash ADC. From the resolution point of view successive approximation resolution that is from 8 to 16 bits is comparable with pipelined structure but the fastest flash has maximum resolution of 6 to 8 bits. Therefore we can conclude that it is always the trade-off between speed, accuracy and power. The selection of architecture is depended upon

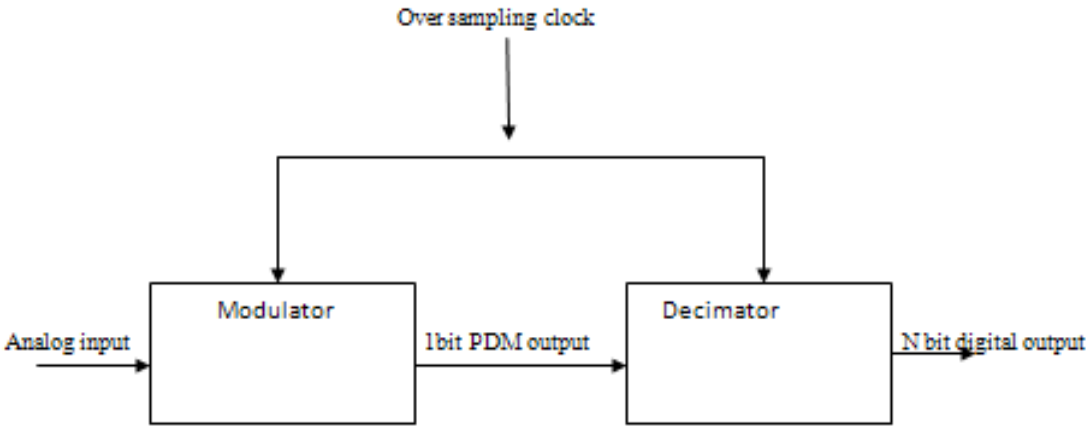
the application.All families of converters are speed up with the CMOS process improvements e.g. successive approximation conversion time has been increased to tens of microseconds. This also effects the power consumption of data converters. On the other hand improvement in DSP functionality also impacts on the ADC design e.g. improvement in sigma-delta converter by adding fast and more complex digital filter.

2.8Sigma Delta ADC

Sigma delta ADC comes under the category of oversampling ADC, which samples the signal at an over sampled frequency of fN=k2F where k is the oversampling ratio and is given by the following equation.

$$K=fn/F \qquad 2.1$$

2.**5**shows the block diagram and description of sigma delta ADC. The modulator part samples the input signal at a much higher frequency set by the over sampling convert which converts the analog input signal to pulse density modulated signal followed by a decimation filter which contains the original input signal and out of band noise.Both the modulator and the decimator are operated with the same over sampling clock. The modulator is of first order with a 1-bit quantize and it generates a 1-bit output. The output of the decimator is N-bit digital data, where N is the output resolution of the ADC and is dependent on the over sampling ratio of the converter.



2.5 Block diagram of a sigma-delta analog to digital converter

The following sub-sections below gives anoverview of the terms quantization noise, signal sampling and noise shaping which are related to sigma-delta converters.

2.9Quantization Noise

The analog signal can take any continuous value. But a digital n-bit signal only settles to 2n discrete values. Quantization noise is the difference between the analog value and its digital representation, which causes the distortion .Quantization error, can be defined as a measure of an n-bit converter's failure to represent accurately an analog signal in the digital domain.

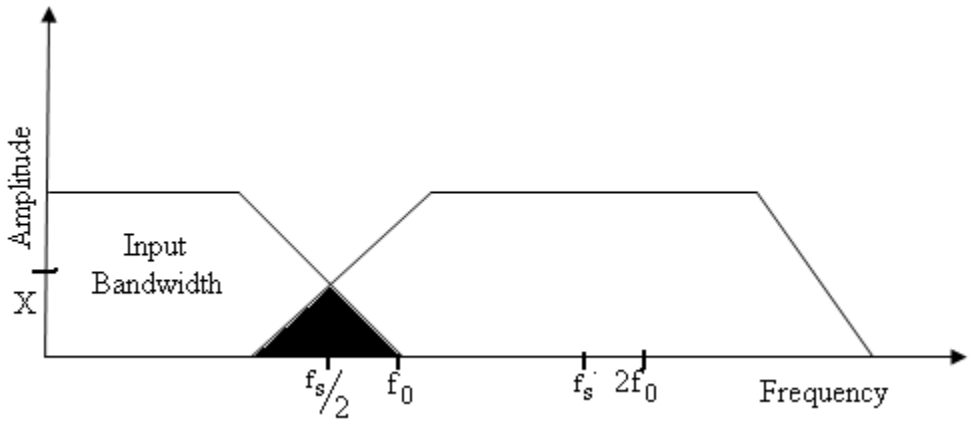
2.10 Signal Sampling

In the process of oversampling the input analog signal is sampled at a much higher frequency then the Nyquistfrequency, which reduces the quantization noise to a great extent in the required band of interest. In order to construct the sampled signal without distortion the sampling frequency must be twice of the signal frequency as stated by the sampling theorem. 2.6shows the spectrum of an under sampled signal[2] Here the sampling frequency, fs is less than twice the input signal frequency 2f. The shaded portion of the figure shows the aliasing which occurs when

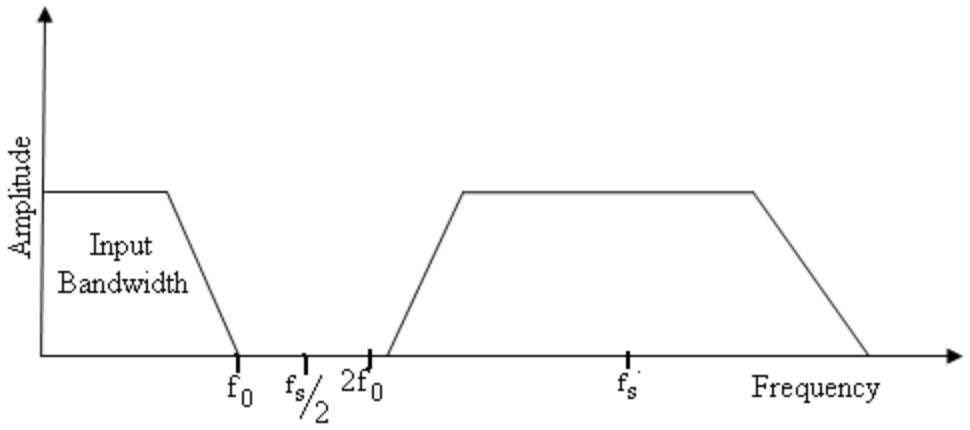
the sampling frequency is not twice the signal frequency. We get a distorted signal at the output **2.7**shows the spectrum of an oversampled signal [2]Here the sampled signal in the frequency domain appears as a series of band-limited signals.This puts the entire input signal bandwidth at less than fS/2 which reduces the aliasing.

2.11 Noise Shaping

It is one of the properties of sigma-delta ADCs which results due to the application of feedback which extends dynamic range. The closed loop modulator works as a high-pass filter for quantization-noise and as a low-pass filter for the input signal. When the signal is over-sampled, the quantization noise power in the Nyquist bandwidth spreads over the wider bandwidth, which is shown in 2.8. The total quantization noise is still the same but the quantization noise in the bandwidth of interest is reduced significantly. The figure illustrates the noise shaping which is achieved by using the oversampled sigma-delta modulator.

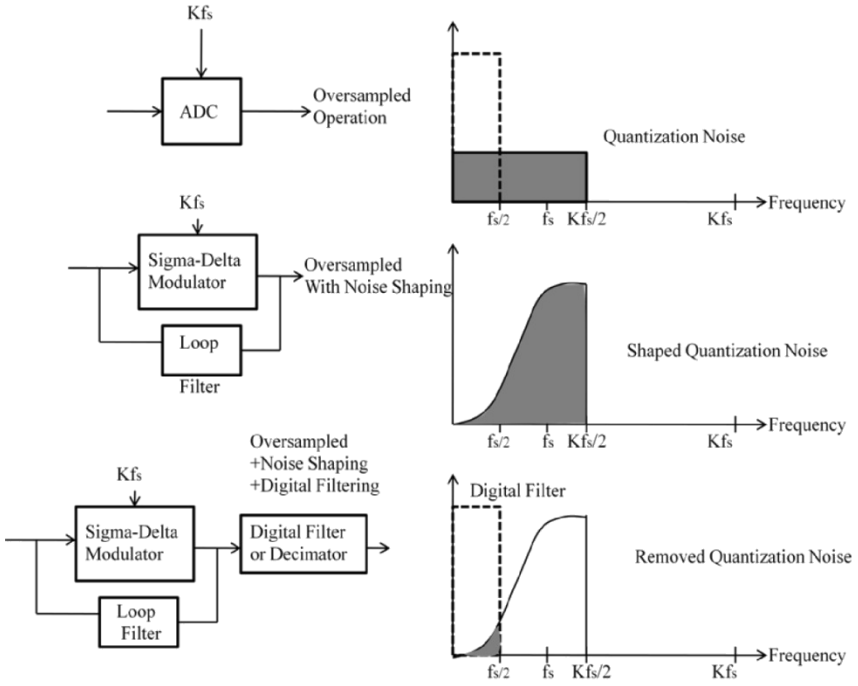


2.6 (a)Under sampled signal



2.7Fig2.6(b) Oversampled signal

In a sigma-delta ADC, the analog modulator samples the input at oversampling ratio and after the input signal passes through the modulator it is fed into the digital filter or a decimator. The digital filter provide a sharp cutoff at the bandwidth of interest, which essentially removes out of band quantization noise and signals



2.8 Putting noise shaping and Digital filter together

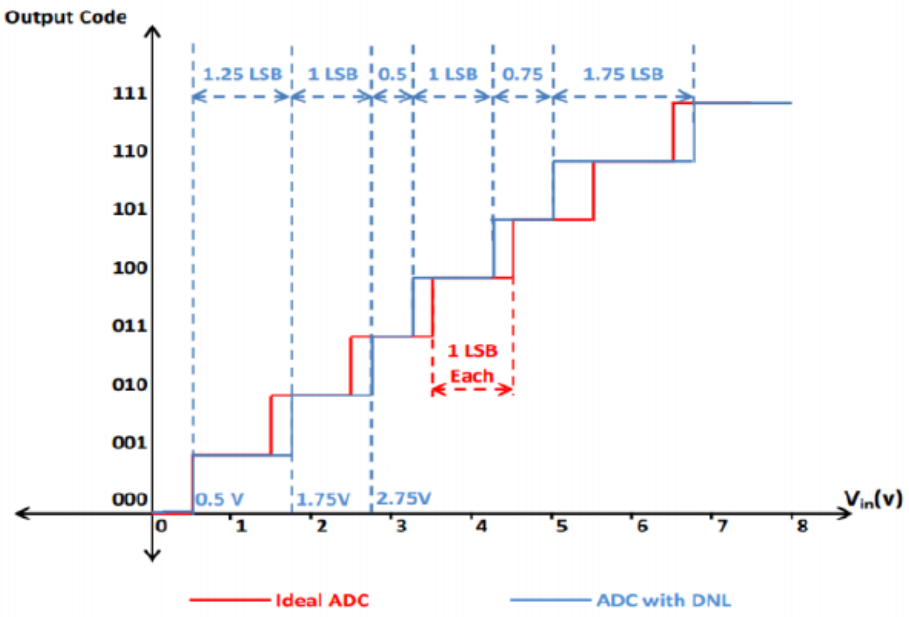
2.12 Spur- Free Dynamic Range (SFDR)

SFDR is the ratio of the strength of the fundamental frequency to the strongest spurious signal in the output of ADCs. SFDR is an indicator of fidelity of an ADC. Non-linearity in the ADC generates spurious signals that affect the achievable SFDR.SFDR can be calculated using the below formula

SFDR=Signal (dB) - largest spur (dB)

2.13 Differential non- linearity (DNL)

DNL is a measure of separation between adjacent levels measured at vertical jump.DNLmeasures any deviation from one LSB. In other words, for an ideal ADC, the output is divided into 2_N uniform voltage levels, each with width. Any deviation from the ideal step width is calleddifferential non- linearity (DNL) and is measured in number of counts (LSBs). The DNL is 0LSBFor ideal ADCs. In a practical ADC, DNL error comes from its architecture. For example, in a SAR ADC, DNL error may be caused near the mid-range due to mismatching of its DAC. Let us consider an example of a 3-bit ADC with transfer characteristics as shown in Fig. In this ADC, each input step should be exactly 1/8 of the full-scale input range (1 LSB of this ADC). Given that this ADC has an input range of 8V, the first output-code transition is caused by an input change of 0.5V (Full-scale input range/16 = ½ LSB), which is as expected. However, the second transition, from 001 to 010, takes place after an input change of 1.25V (1.25 LSB), and so is too large by 0.25 LSB. Similarly, there is a variation in step size at each of the following steps. The DNL of this particular ADC can be specified as 0.75 LSB, which is the maximum deviation from the ideal step size of this ADC throughout its transfer.



2.9 Representation of DNL in an ADC transfer curve

2.14 Integral non-linearity (INL)

Integral non linearity (INL) is the maximum difference between actual finite resolutioncharacteristic and ideal finite resolution characteristics. In the other words INL is a measure ofhow closely the ADC output matches its ideal response. INL can be defined as the deviation inLSB of the actual transfer function of the ADC from the ideal transfer curve. INL can be estimated using DNL at each step by calculating the cumulative sum of DNL errors up to that point. In reality, INL is measured by plotting the ADC transfer characteristics as explained below. There are two methods to find the INL error

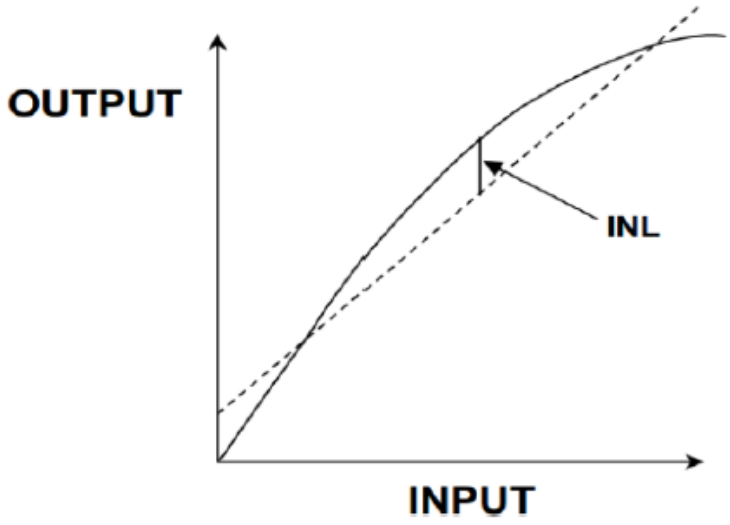
1. Best fit (best straight line) method

2. End point method

Best fit (best straight line) method

The best fit method of INL measurement considers offset and gain error. One can see in 2.10that the Ideal transfer curve considered for calculating best-fit INL does not go through the origin.

The ideal transfer curve here is drawn such that it depicts the nearest first-order approximation to the actual transfer curve of the ADC. The intercept and slope of this ideal curve can lend us the values of the offset and gain error of the ADC. Quite intuitively, the best fit method yields better results for INL.

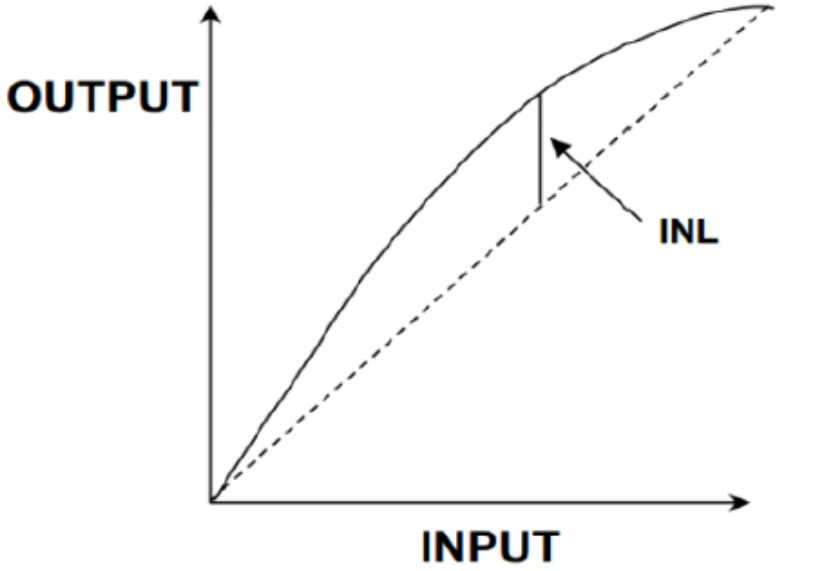


2.10 Best fit INL

The only real use of the best fit INL number is to predict distortion in AC applications. This number would be equivalent to the maximum deviation for an AC application.

2.15 End-point INL:

The End-Point method provides the worst case INL. This measurement passes the straightline through the origin and maximum output code of the ADC. As this method provides the worst case INL, it is more useful to use this number as compared to the one measured using best fit for DC applications. The parameter INL must be considered for applications involving recession measurements and control.



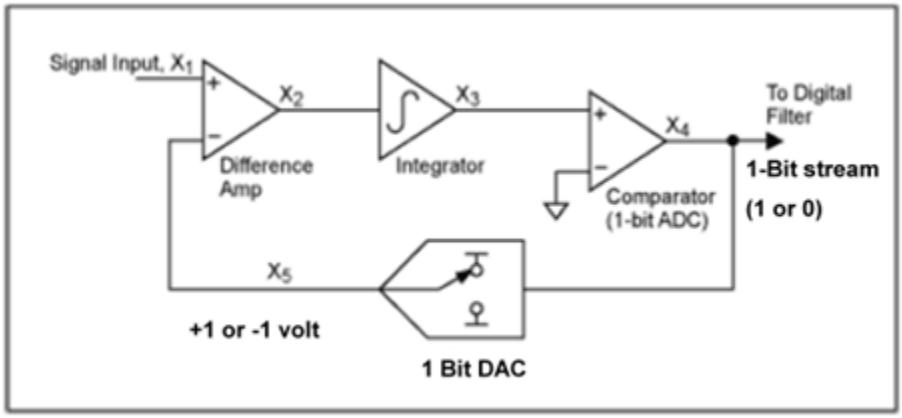
2.11 End Point INL

2.16 MODULATOR

The modulator is the analog part of sigma delta ADC, the resolution of the converter depends upon the order of the modulator order of the modulator is set by the sampling ratio. It consists of an integrator and a comparator (ADC) in the forward path and a DAC in the feed backpath, Delta is used to show deviation or small incremental change known as “delta modulation”. it is based on quantizing the change in signal by sample to sample rather then absolute value of signal at each level. Sigma or integrating is done at the input side of the converter of the output of DAC and the input signal. So this modulation is called as sigma delta modulation. The feedback signal from the DAC is subtracted from the input signal by the summing amplifier, and then the error signal is filtered by the low pass filter integrator. The comparator works as at oversampling clock frequency and act as quantizeror ADC. It compares the input signal against last sample signal to see if it is higher then the reference or not. if it is larger then the output is increased else

decreaced.The density of ‘1s’ and ‘0s’ forming a pulse stream at the output is the digital representation of the input analog signal. A converter needs a sampling frequency more then twice the signal frequency to reproduce the signal without distortion. The density of the pulses represents the average value of the input, most of the pulses are high for the positive peak of analog signal and the density of negative pulses represents the negative peak of the signal.

By balancing three major design aspects the resolution of the sigma delta ADC can be increased they are the over sampling ratio, quantizer resolution and order of modulator. The use of a higher order modulator reduces the superimposed noise in the bit stream. The in band quantization noise can be reduced by doubling there sampling frequency. The input analog signal can directly be sampled using an input over sample clock as it uses the process of oversampling this also eliminates the use of antialiasing filter due to oversampling process.



2.12 Block diagram of modulator

The modulator consists of an Integrator, Difference Amplifier, 1bit latched Comparator (ADC) and a 1bit DAC.**2.12**shows the basic structure of a modulator. The modulator pushes the output of the modulator to a higher frequency range which can be filtered using a digital decimation filter.

2.17 DECIMATOR

Decimation is the process of converting the sampling rate of a signal from a given higher rate fs tolower rate f_n.Decimation means reducing by a factor 10.but in communication it is the reduction in the sampling rate of the signal. It is a digital low pass filter which performs the samples rate reduction operation. The sigma-delta modulator performs the operation of noise shaping and hence the noise is pushed to higher frequencies so that the decimation stage following the modulator can filter out this noise above the cutoff frequency. The band limited signal can then be resample by discarding K – 1 samples out of every K samples, where K being the oversampling ratio. By averaging K samples out of the quantized sigma-delta output, the decimation filter achieves a high output resolution and also the frequency of the output data is at twice the input signal bandwidth which is the nyquist rate.

3. Designing of Sigma Delta ADC

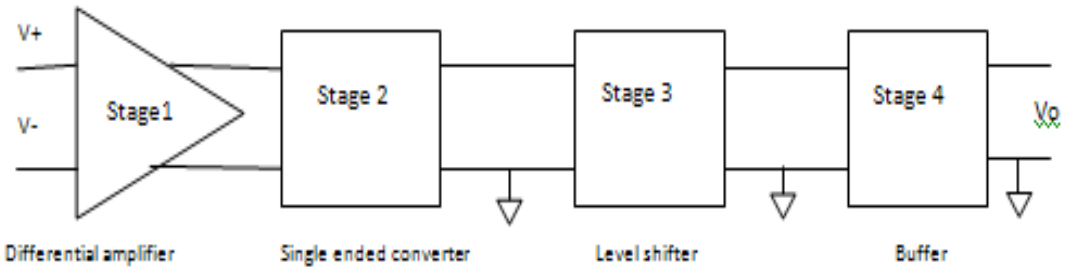
As stated above in chapter 2, The Sigma Delta ADC basically divided into two parts. One is the modulator part and the other is the decimator part. As shown in Fig.2.11, the input analog signal is given to the modulator part where the oversampling ,quantization and noise shaping process is carried out and the results in a pulse stream of digital output. This is given to the decimation filter which decimates higher frequency over sampled signal from the modulator to lower frequency signal; itfilters out the noise above the cutoff frequency range. The following chapter describes the designing requirement and parameters of the different sub modules that are required for designing a modulator and the filter.

The basic architecture of Sigma Delta Modulator as shown in the above figure2.11 consists of a differential amplifier, an integrator a comparator and a DAC in the feed back loop of the modulator.

3.1 Designing of Operational Amplifier

One the most commonly used device in analog world is operational amplifier (OP-Amp), It is a device whose output can be easily related to input in terms of some known mathematical equations and operations. By using some active and passive elements like resistors and capacitors in integrator and differentiator circuits this can be achieved. An Op-Amp can be characterized by high input impedance, high gain margin, low output impedance, high band width. It has also the ability to amplify the differential mode signal to a high extent and attenuates or rejects the common mode signal. Basically an Op-Amp mainly consists of four different functional blocks likely, the differential gain stage, the single ended conversion stage, thelevel shifting stage and finally the buffer stage. In the first stage that is the differential gain stage, amplifies independently there average and common mode signals. It is one of the most critical and important stage of an Op-Amp, it decides some of the most important parameters like

Common mode rejection ratio (CMRR), common mode input range (ICMR) and the input noise. The second stage that is the single ended conversion stage which is present after the differential stage is responsible for giving a single ended output which is referred with the ground. The next is the level shifter stage which is introduced after the single ended conversion stage and finally the buffer or the second gain stage which provides the necessary gain to the amplifier.3.1shows the block diagram of basic integrated Op-Amp.

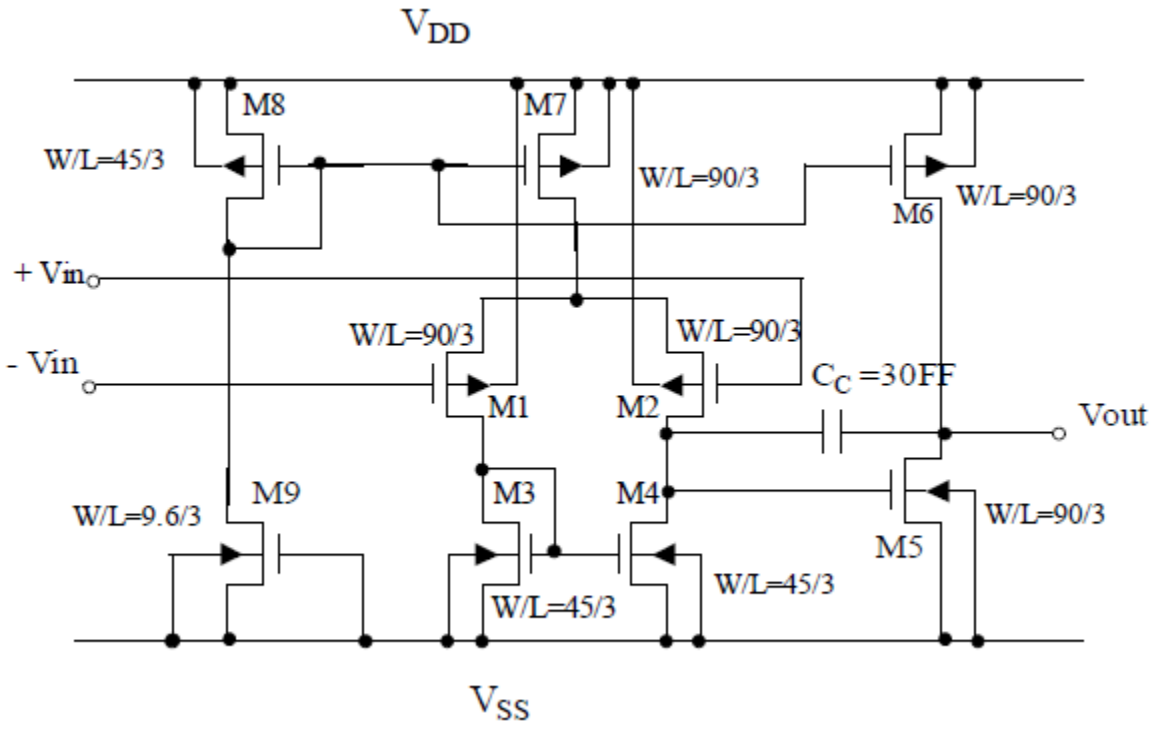


3.1 Block Diagram of Basic Integrated Op-Amp.

3.2 Two stage CMOS Op-Amp Topology

Two stages Op-Amp configuration shown in Fig 3.2 is one of the most widely used operational amplifier. It provides a good common mode range, good voltage gain and a good output swing. Some of the basic principle behind the operation of Op-Amp is, a differential pair of p-MOS transistor (M1, M2) is used to implement the input differential amplifier stage. Where there sources are tied together. It is biased with a current mirror which acts as a load circuit. In order to increase the common mode rejection ratio (CMRR) of the Op-Amp two current mirror circuits (M7, M8) which is p-MOS circuit and (M3, M4) n-MOS circuit are use instead of only

one. The p-MOS current mirror circuit serves the purpose of a constant current source and the n-MOS serves as an active load as it sinks current. The first stage output is taken across this n-MOS terminal there by performing a differential to single ended conversion.



3.2 Two stages Op-Amp configuration

3.3Current Mirror

These are used extensively in analog MOS circuits both as active load elements and biasing circuits to get a high AC voltage gain (3, 4). It is one of the basic building blocks in CMOS IC design and is used for analog circuit designs. The output impedance of this should be infinite and it should be capable of drawing or generating constant current over a wide range of voltages. As the gate is tied to the drain enhancement mode transistor will remain in

saturation. Due to thresh hold voltage drop drain to source voltage (V_{DS}) will always be greater then gate to source voltage (V_{GS}).

$$V_{DS} > V_{GS} - V_T \qquad (3.1)$$

Basedon equation 3.1,a constant current mirror is achieved by supplying a reference current through a gate tied to drain (i.e. diode connected) transistor. The p-MOS current mirror serve as current source and the n-MOS serve as current sink. As shown in Fig.3.3 and Fig.3.4.The voltage developed across the diode connected transistor is applied to the gate and source of the second transistors provides a constant output current. When both the transistor is in saturation region of operation, both of them will have same gate to source voltage. During this region of operation the transistor are governed by the following equations (3.2) and (3.3).Assuming transistors are in match, the current ratio I_{OUT}/I_{REF} is determined by the aspect ratio of the transistors.

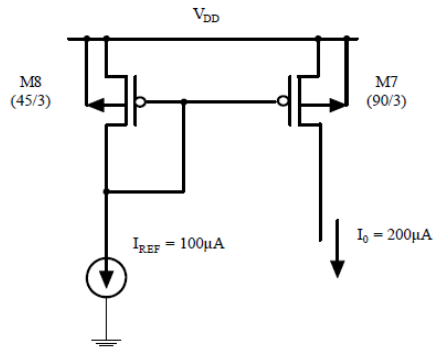
For p-MOS current mirror we have

$$I_{OUT}/I_{REF} = (W_7/L_7)/ (W_8/L_8) \qquad (3.2)$$

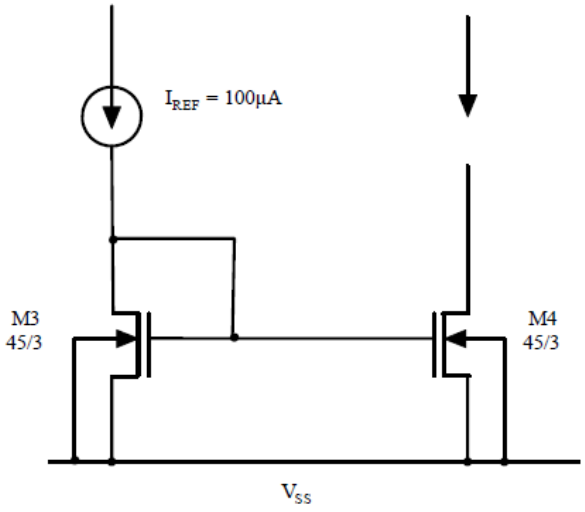
The ratio is unity for identical size transistors, so the output current mirror's the input current.

For n-MOS current mirror design we have

$$I_{OUT}/I_{REF} = (W_4/L_4)/(W_3/L_3) \qquad (3.3)$$



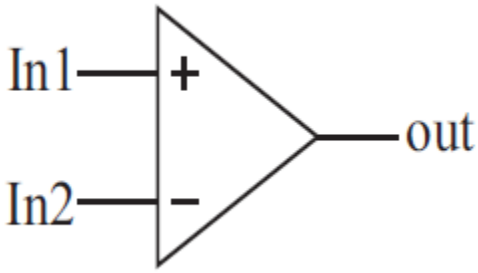
3.3 p-MOS current mirror design



3.4 n-MOS current mirror design

3.4Designing of Comparator

A comparator is a circuit that performs the operation of comparing two analog input signals and decoding the difference in to a single digital output signal.3.5shows a basic comparator symbol.

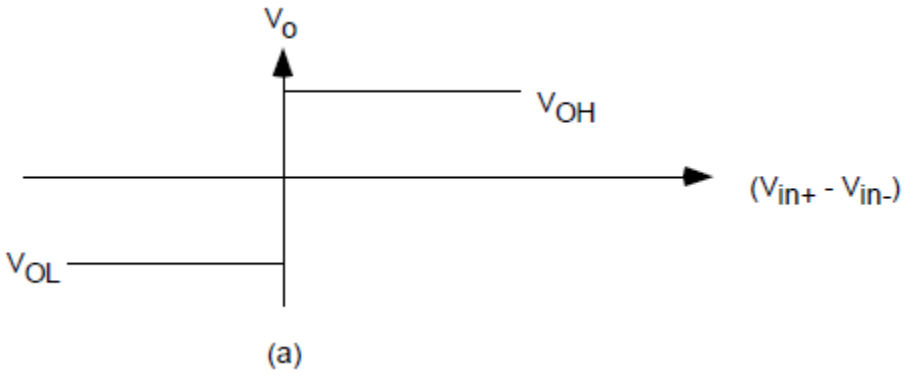


3.5 Comparator Symbol.

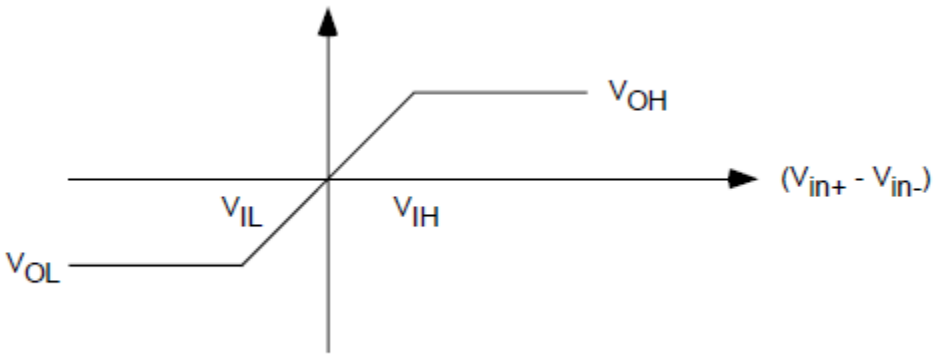
The comparator is one of the most critical parts of almost all analog-to-digital (ADC) converters, Depending up on there size and structure they can have a severe impact on the performance of a device. The speed and resolution of an ADC is directly affected by the input offset voltage, the delay and input signal range (5).Comparators are classified

depending upon therenature, functionality and inputs. Like voltage and current comparators, continuous and discrete time,etc.Some of the basic application of comparators is analog-to-digital conversion, functiongeneration, signal detection and neural networks etc.

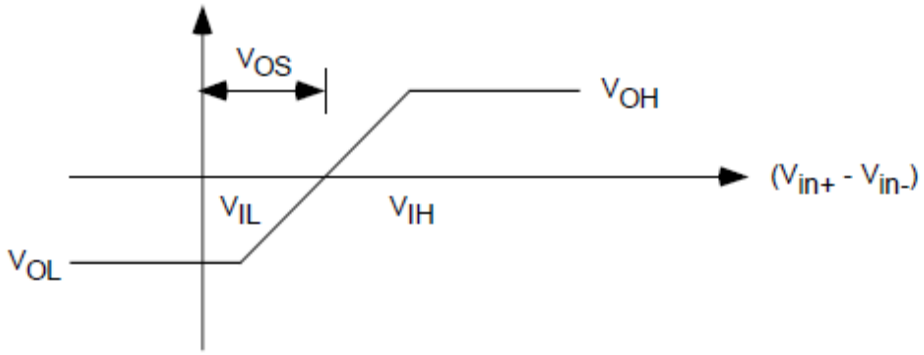
The comparator takes the analog input and gives a binary or digital output as shown in 3.6



(a)



(b)



(c)

3.6 (a), (b), (c) different outputs of comparator

Fig.3.6 (a) defines as follows

$$V_o = \begin{cases} V_{OH} & \text{if } V_{in+} - V_{in-} > 0 \\ V_{OL} & \text{if } V_{in+} - V_{in-} < 0 \end{cases}$$

This is not realizable as its gain is infinity. Fig.(b) Shows a realizable first order characteristic of a comparator, its output is defined as follows.

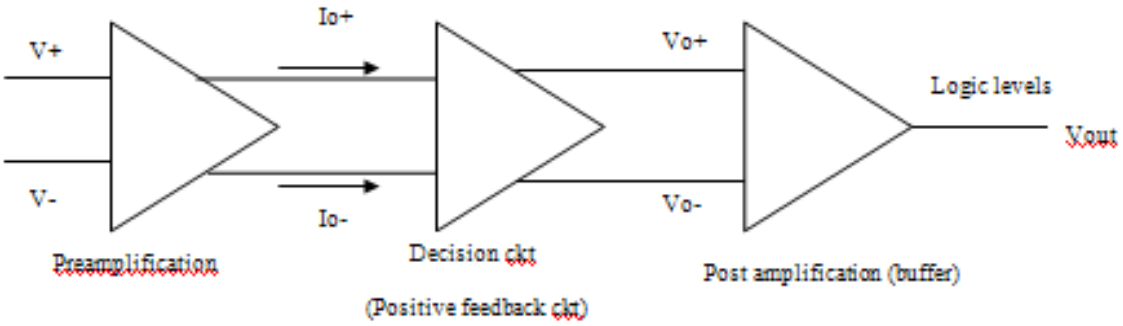
$$V_o = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V (V_{in+} - V_{in-}) & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

One of the non ideal characteristic of comparator is presence of input offset. That is the output does not change until the difference input reaches the input offset Vos.Fig. (c) Showsthese characteristic' of the output which defines as follows.

$$V_O = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V(V_{in+} - V_{in-}) - A_V V_{OS} & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases}$$

Here the input offset can be removed or ignored by proper layout.If the input is sufficiently small then the output will not slew and the transient response will be a linearone. Thesettling time is defined as the time needed for the output to reach a final value within a determined tolerance, when excited by a small signal. The settling time of small signal is determined by the gain bandwidth product of the amplifier. If the input magnitude issufficiently large then the comparator will slew by virtue of not having enough current to charge or discharge the compensating or load capacitor. The slew rate is determined from the slop of the Outputs wave form during the rise or fall of the output. It is limited by the current sourcing or Currentsinking capability in charging the output capacitor. Settling time is very important in analog signal processing. It is very much necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of processing the analog signal. A longer settling time indicates the reduction in the rate of processing analog signal.

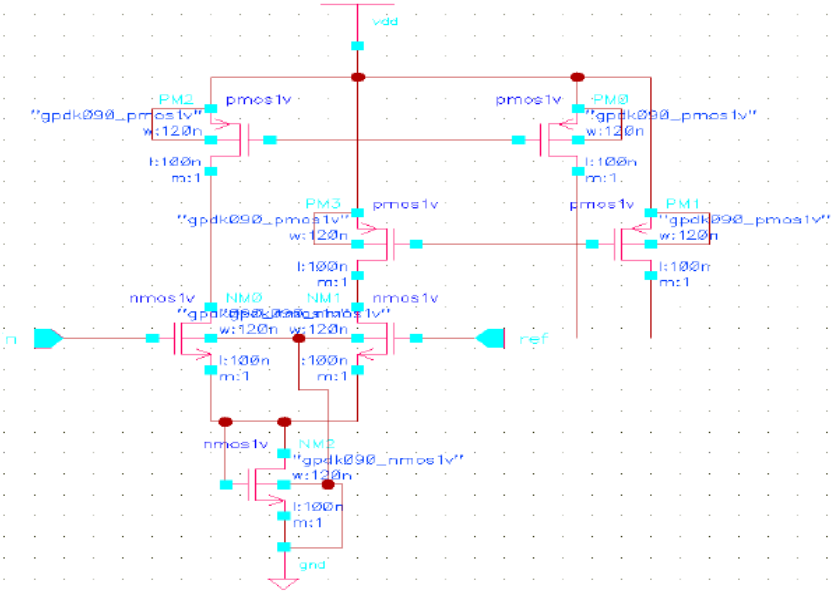
A block diagram of a high performance comparator is shown in 3.7.It consists of three stages ,The preamplifier stage, that amplifies the input signal to improves the comparator sensitivity and isolates the input of the comparator from switching noise coming from the positive feedback stage(second stage) . This is used to determine which input signal is larger. The last stage is the output buffer stage which amplifies the information and gives a digital signal.



3.7 Block diagram of a voltage comparator.

Preamplifier

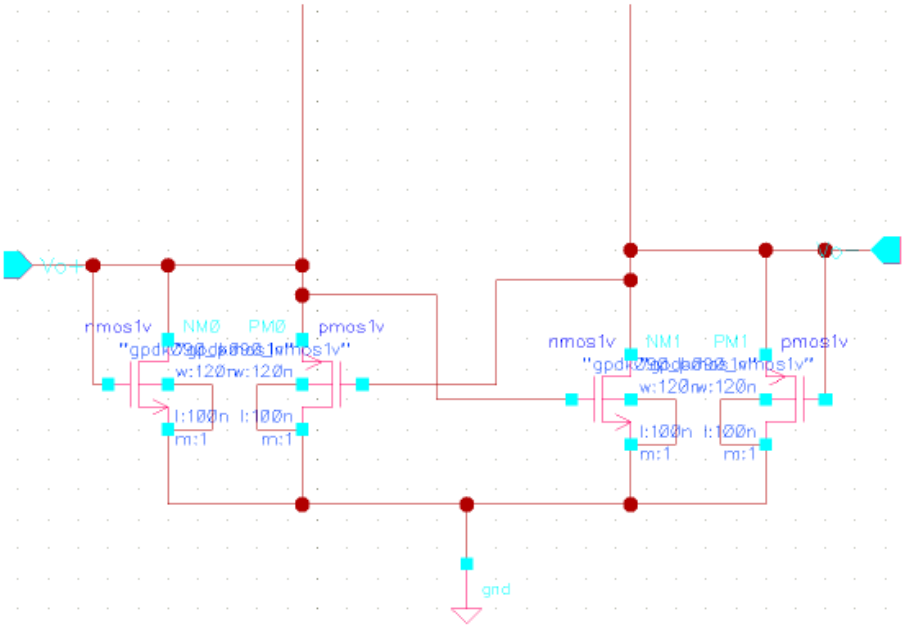
The preamplifier is a circuit which is used to amplify the signal so that it can easily drive load. in most latch comparator circuit preamplifiers are used to avoid the kickback effect from latch and input referred offset (6) The preamplifier stage, that amplifies the input signal to improves the comparator sensitivity i.e. increase the minimum input signal with which the comparator can make a decision.



3.8 Schematic of preamplifier

Decision Circuit

The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals; we should be able to design the circuit with some hysteresis for use in rejecting noise on a signal. It uses positive feedback from the cross gate to increase the gain of the decision element3.9shows the schematic of decision circuit.

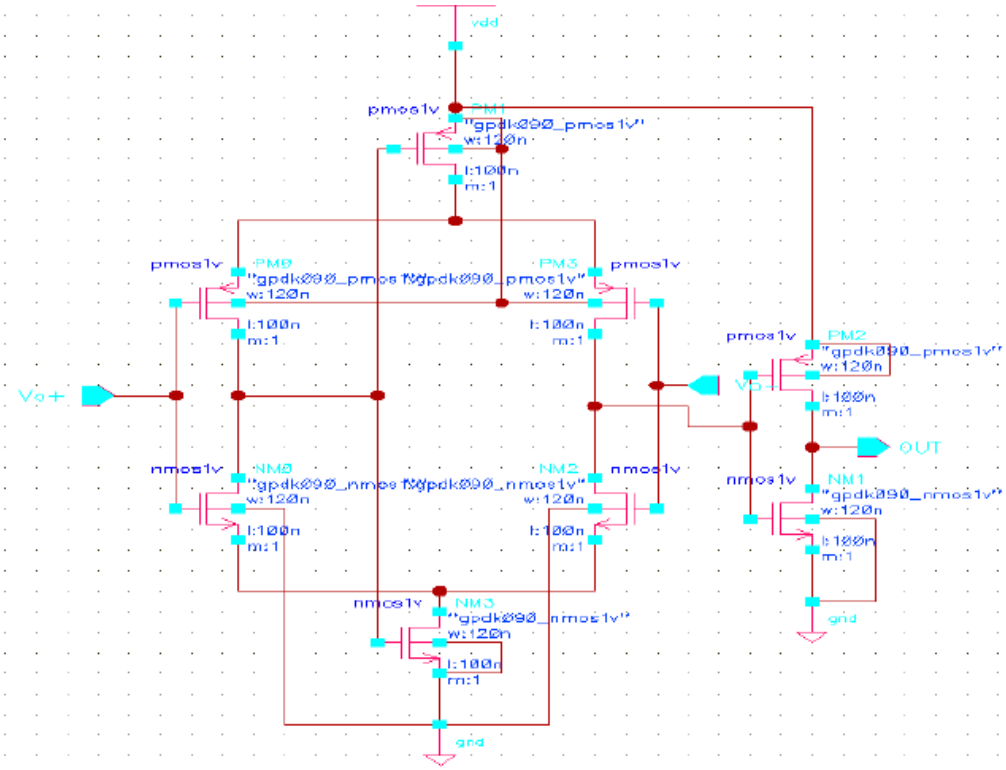


3.9 schematic of decision circuit

Output Buffer

The circuit used as an output buffer is a self biasing differential amplifier. An inverter was added on the output of the amplifier as an additional amplifier. The final component of the comparator design is the outputs buffer or post amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into logic high or low. The output buffer should accept a

differential input signal and not have slew rate limitation.3.10shows the schematic of output buffer.



3.10 Schematic of output buffer.

3.5 Designing of Latch Comparator

Dynamic Latch

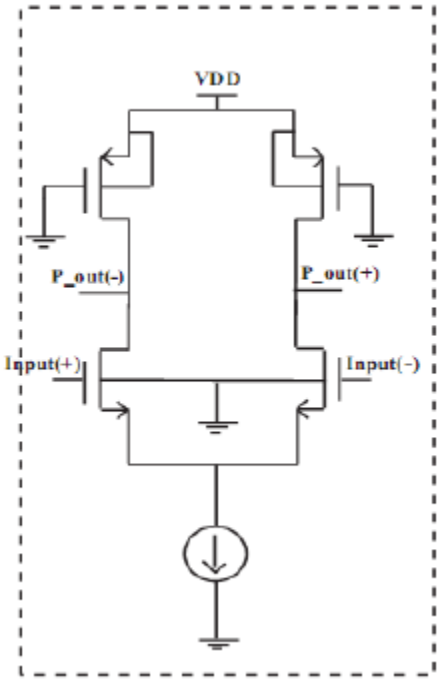
It is defined as the memory unit which stores the charge at the gate capacitance of the inverter. A symbol of dynamic latch is shown in Fig3.11 below.

The above circuit is driven with a clock signal. During the active phase of the clock (clk=1), the transmission gate is closed and the latch acts transparent where as the inverter is directly connected to the input. During the other phase (clk=0), the transmission gate is open and the

output of inverter is determined by the node. In order to ensure proper operation of the latch the setup time and hold time must be taken in to consideration which is determined by the transmission gates.

Preamplifier

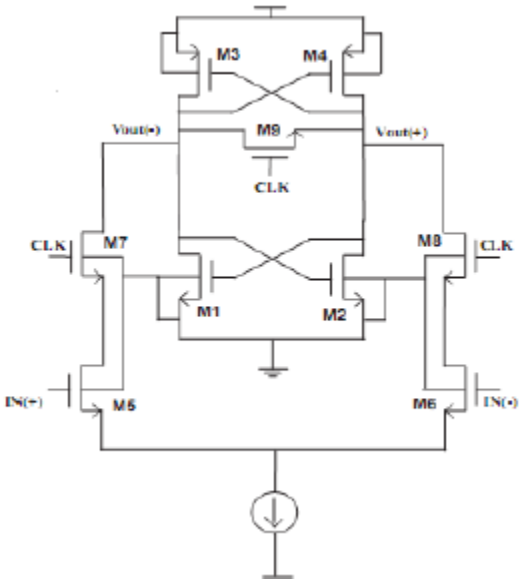
The preamplifier used in latch comparator is a common mode differential amplifier with p-MOS as the active loads. This is followed by a small kick back circuit which is used for two main purposes. First it helps to avoid the kick back effect from latch by using two n-MOS transistors operating on a clock. Secondly the kick back circuit helps in creating charge imbalance in the circuit when it switches from reset to regeneration mode.Fig.3.11 shows the basic schematic structure of a preamplifier.



3.11 structure of preamplifier

3.6 Comparator Architecture

Here the comparator uses a regenerative structure of a dynamic latch. The circuit consists of two inverters connected back to back forming a differential comparator, the comparator uses the regenerative structure of a dynamic latch. It consists of two inverters connected back to back with each other forming a differential comparator and an NMOS transistor is connected between the two differential nodes of the latch.Fig.3.12 shows the structure of a comparator circuit.



3.12 structure of Comparator

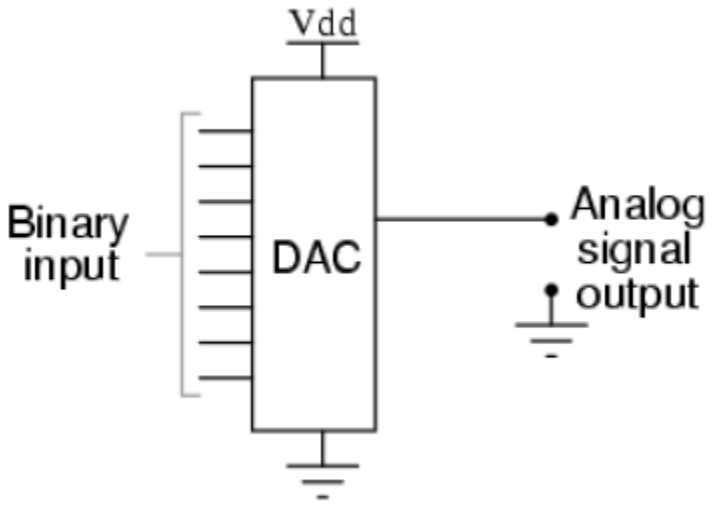
Comparator Operation

In the above circuit the comparator senses the charge imbalance produced at the preamplifier in the input and reacts to the imbalance so as to create desired digital output. It can also be called as current comparator. The total operation of the comparator is divided into two phase. When the clock is high, the transistor acting as switch closes and short circuits the outputs and set them to a certain DC level around Vcc. In same phase the preamplifier causes charge imbalance at the

differential node of latch. In the other phase, the short circuiting transistor is switch off and the preamplifier is also disconnected. In this phase the comparator, amplifies the charge imbalance to digital voltage level at the differential node.

3.7Designing of Digital-to-Analog Converter(DAC)

It is a device for converting a digital usually binary code to analog signal (current, voltage or charges).The DAC acts as an interface between digital world and analog real world. The DAC inputs a digital signal and outputs an analog signal in form of current, voltages or charges.Fig.3.13 shows the basic symbol for a DAC.



3.13 Basic symbol of DAC.

Types of DAC Circuits

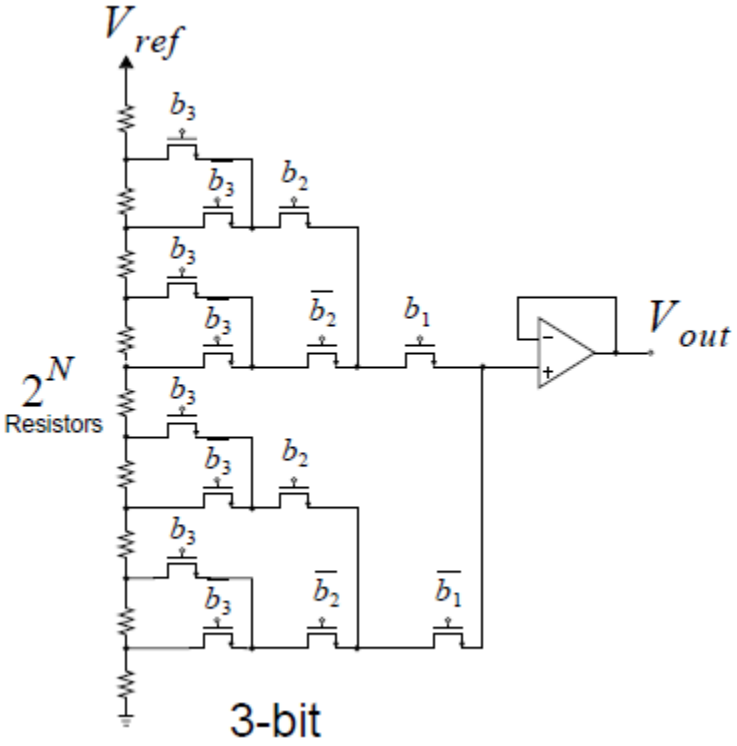
Resistor-String

N-Bit Binary Weighted Resistor

R-2R Ladder

Resistor-String

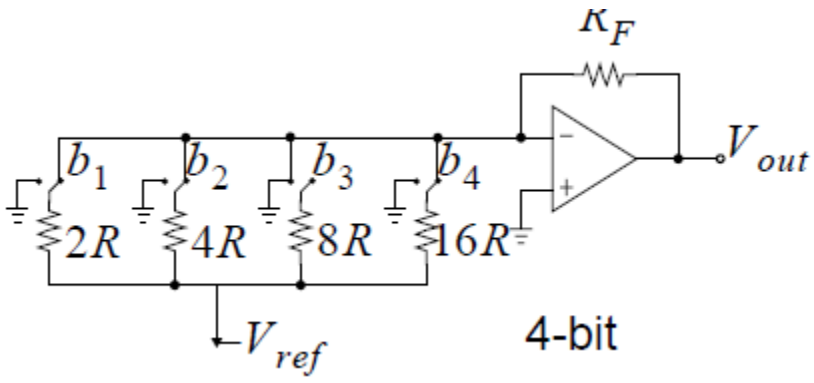
These types of DAC are used for guaranteed monotonic. The major speed limitation is due to the Delay through the Switch network, The resistor present in the circuitry can also be realized using polysilicon.Itrequires 2N resistors, It is mostly integrated with better then 10bit accuracy.3.14shows the basic structure of Resistor string DAC>



3.14 Resistor-string DAC

N-Bit Binary Weighted Resistor

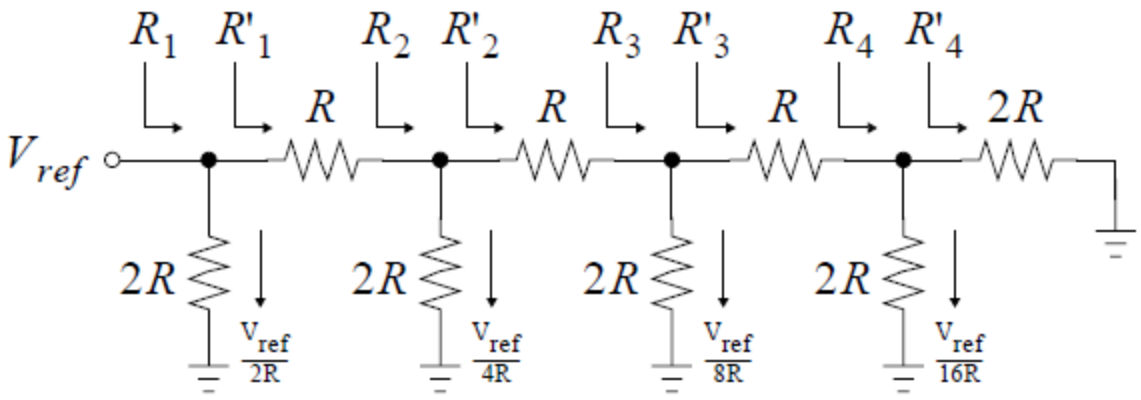
This type of DAC uses only N resistors, here the monotony is not guaranteed, later it is prone to glitches, and the resistor and current ratio are of 2N order. The 3.15below gives the circuit of a N- bit binary weighted DAC



3.15 Binary Weighted DAC

R-2R Ladder

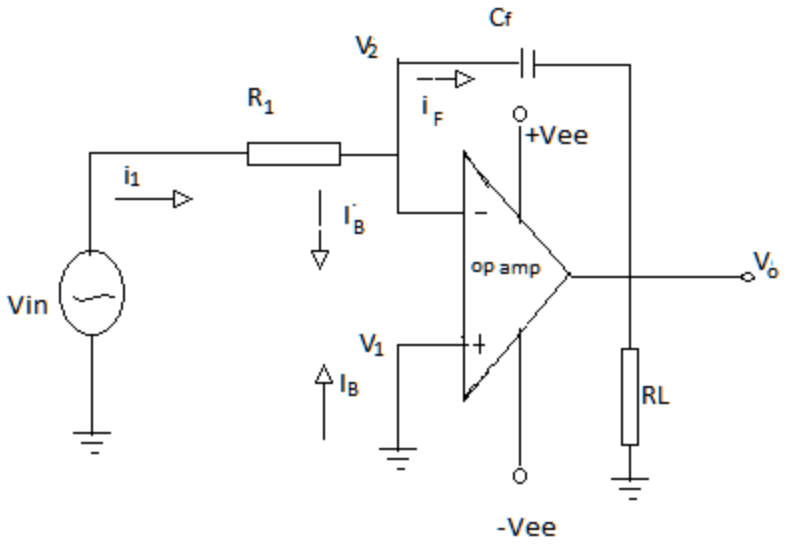
It is one of the simplest types of DAC, it consistsof two precession resistor R and 2R.current through the switches is scaled for good accuracy. It is one of he most widely used DAC.Fig.3.15 show the structure of R-2R ladder DAC.



3.16 R-2R ladder DAC.

3.8Designing of Integrator

As the name implies, the Op-Amp Integrator is an operational amplifier circuit which performs the mathematical operation of integration. It acts like a storage element which produces an output voltage proportional to the integral of its input voltage with respect to time. When a voltage VIN is applied to the circuit the capacitor is little resistance and act like a short circuit giving voltage gain of less then one. No current flows in to the amplifier, as the feedback capacitor begin to charge up, its resistance decreases this result in producing an output voltage that continues to increase until the capacitor is fully charged. At this time the capacitor acts like an open circuit, which blocks the further flow of Dc current. The ratio of feedback capacitor to input capacitor now results in to infinity gain.The rate at which the out put voltage changes or increases is determined by the value of resistor and capacitor, by changing this RC time constant value either by changing value of "C" or by changing value of "R".The time by which it takes to reach the saturation can be changed.Fig.3.16 shows the basic circuit of an integrator.



3.17 circuit of integrator

3.9Designing of Summing Amplifier

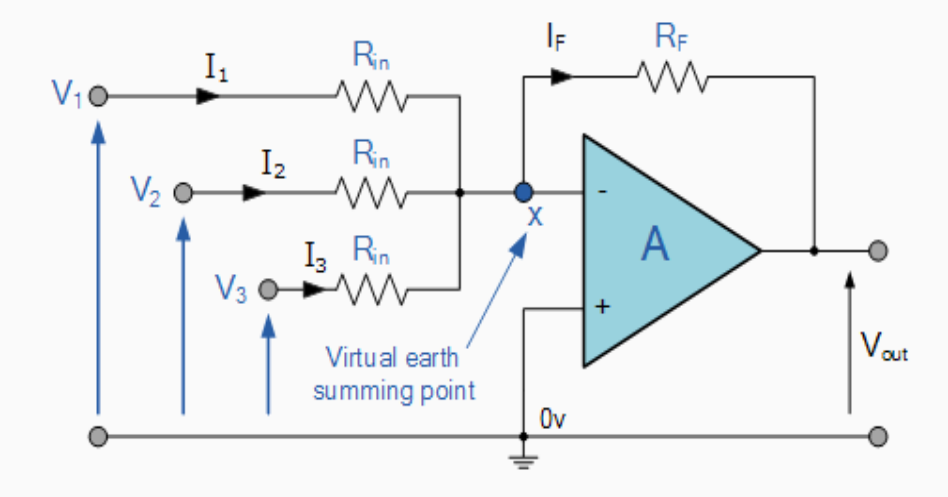
The summing amplifier is a very flexible circuit based on the standard operational amplifier, which can be used for combining multiple inputs. it has a single input voltage applied to the inverting input terminal. If more resistors are added to the input equal to the input resistor, we end up with another operational amplifier called as summing amplifier.3.18shows the circuit of a summing amplifier.

The output is now proportional to the sum of all the input voltages V1, V2 &V3.

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$



3.18 Basic circuit of Summing amplifier.

The above all the basic blocks like integrator,summing amplifier,comparator and the DAC are integrated together to design the Sigma Delta ADC architecture,Which is being given I by a input analog signal and results in a series of discreate digital pulse stream of data.

4. System level Design of Sigma Delta ADC

Design of Sigma Delta ADC

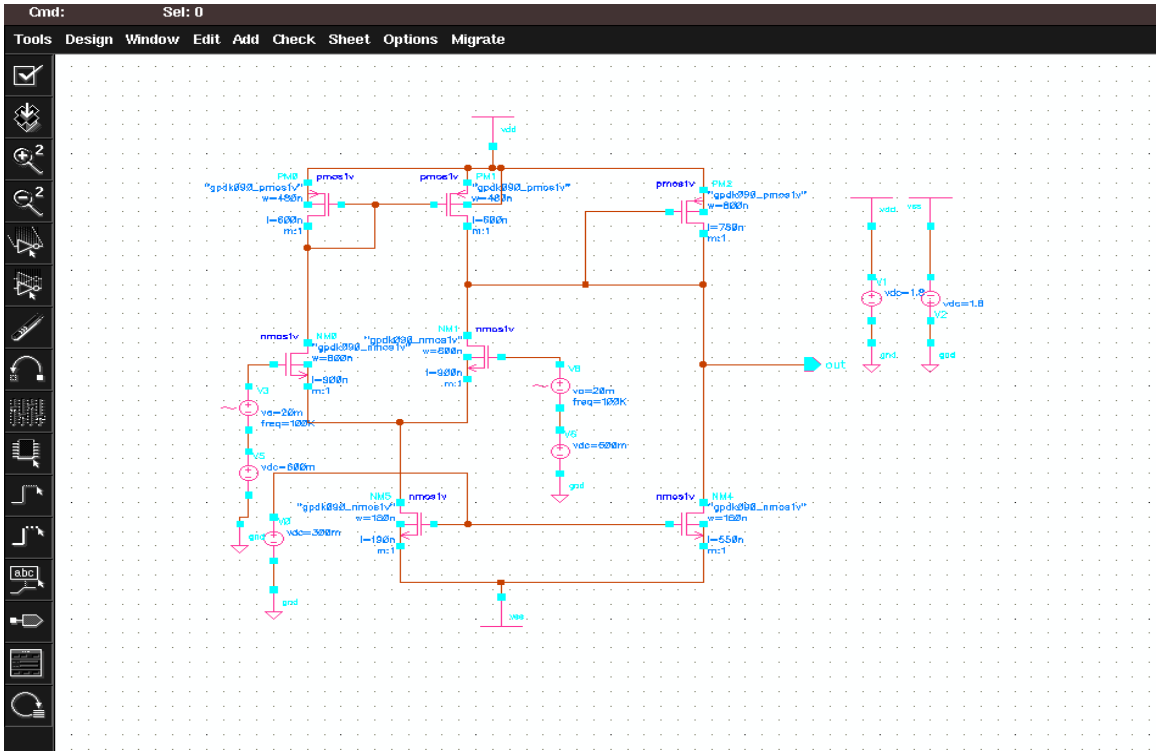
Sigma delta ADC as shown in figure2.1, consist of a Modulator and a Decimation filter. In this report designing of sigma delta ADC is implemented in 90um CMOS technology. The modulator runs on a supply voltage of 1.8v, and achieves a SNR of 85dB for a signal band width of 20 KHz. It operates at an oversampling ratio of 64 and a sampling frequency of 2.56 MHz.

4.1. Designing of Sigma Delta Modulator

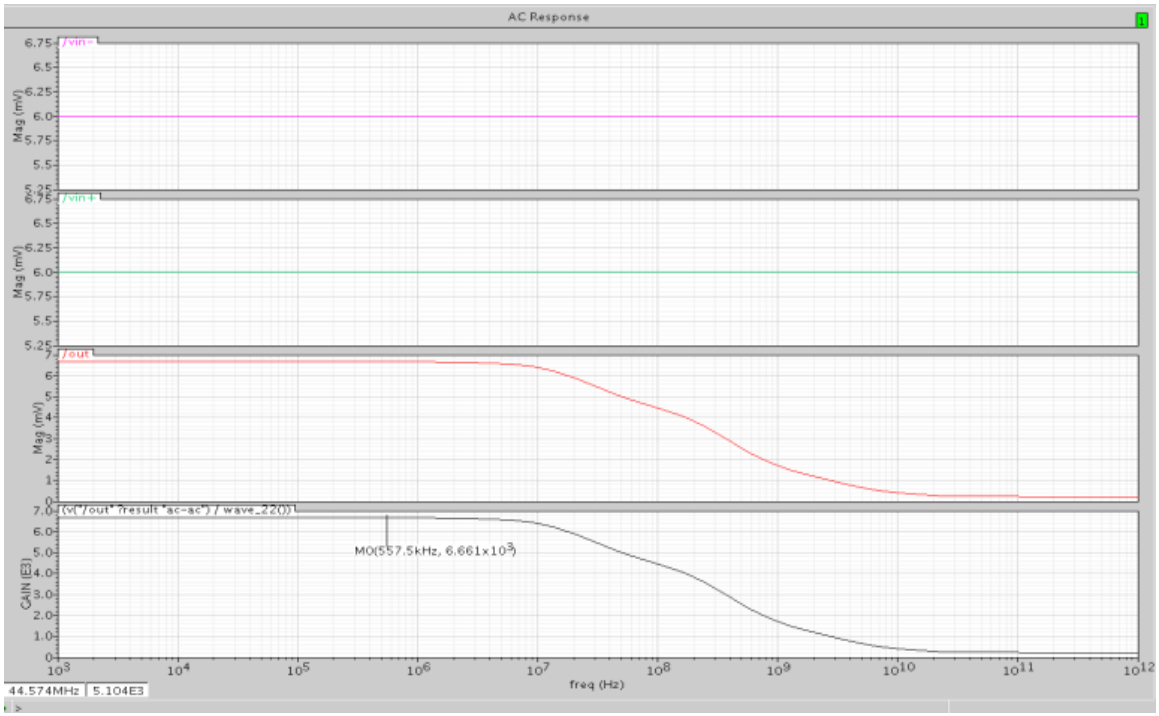
The Modulator as shown in Figure 2.3 consists of a single stage integrator, a summing amplifier, aquantizer(comparator) and a 1bit DAC.The basic building block of this modulator is a simple two stage differential Op-amp.

4.2. Designing of two stage Op-amp

The Op-amp which is the key component of ADC is used by integrator must have high gain to integrate smoothly, with a large bandwidth to pass all harmonics as it is integrating high frequency sinusoidal signal, the unit gain band width must be greater than one clock frequency to pass the signal effectively. The Op-amp used for the ADC 4.1it uses a dual polarity power supply (VDD, VSS) so that the signal can swing above and below the ground. The simulation is carried out by supplying a bias voltage of 0.5v and supply voltage of (1.8 v to -1.8v) and 1 KHz frequency. The open-loop gain of Op-amp was found to be 96db and a gain bandwidth of 57 MHz, the frequency response is shown 4.2



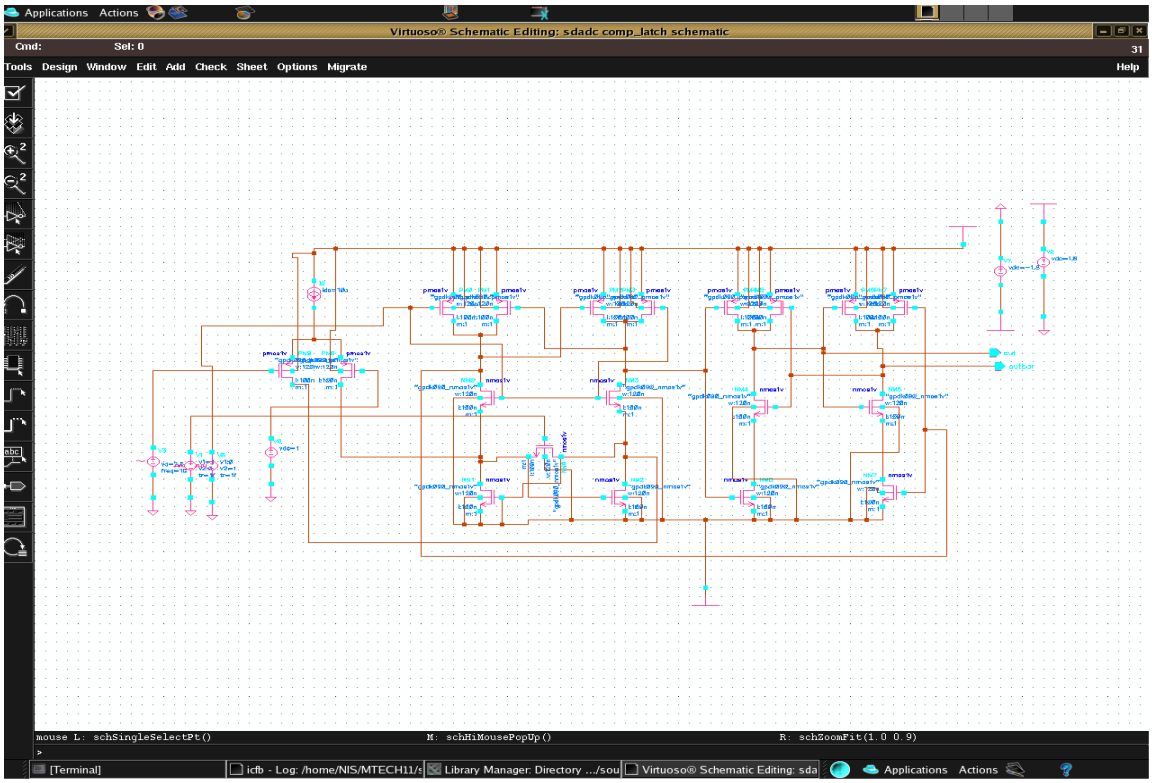
4.1 Schematic of Op-amp



4.2 Frequency response of Op-amp

4.3. Designing of Comparator

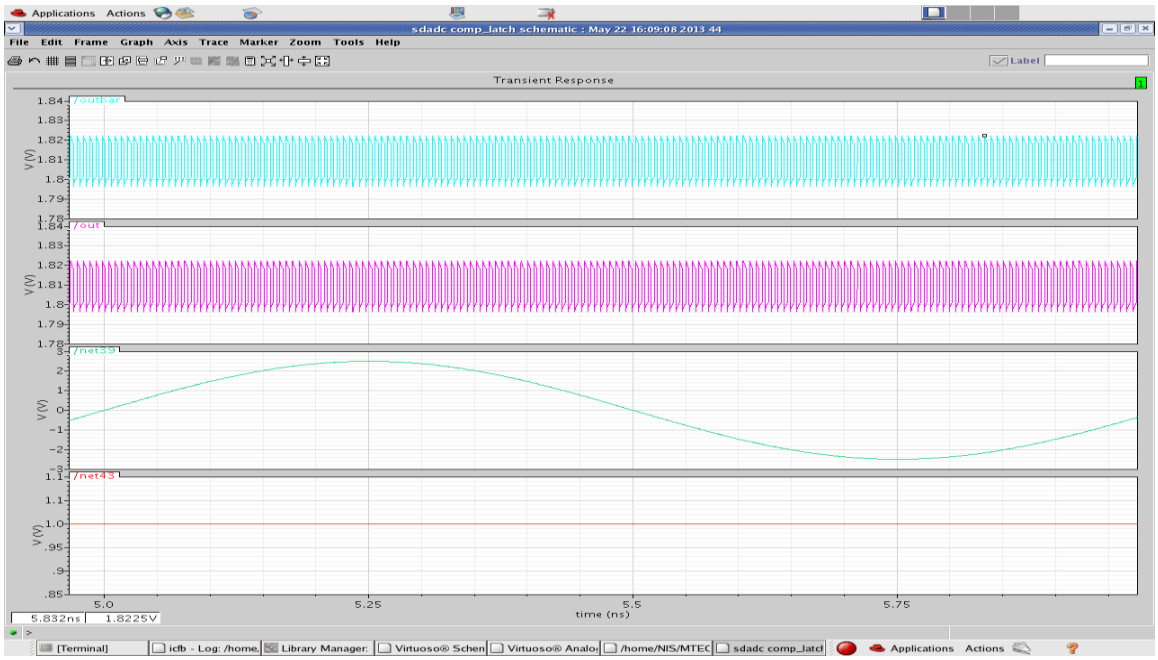
Comparator or quantizer is one of the core components of any analog-to-digital converter (ADC) as we know Nyquist converters need precise analog components in their conversion circuits. Typically, aquantizer design includes a very precise sample-and hold circuit and a high-accuracy comparator working at Nyquist sampling frequency. The accuracy requirement of the comparator depends on the accuracy requirement of the converter, in Σ-Δ modulators, the comparator is required to work at a high oversampling frequency but its resolution can be as small as 1 bit. Therefore, the comparator designing Σ-Δ modulators focuses more on a high-speed operation instead of accuracyand uses a complementary comparator with latch or latched comparator followed by a buffer which helps in buffering the output of the comparator;**4.3**shows the basic schematic of a latched comparator.



4.3 Schematic Design of latch-Comparator

The latch- comparator is simulated using a sinusoidal input signal to the differential pair in its one terminal and making the other ground, two non-overlapping and complementary clock signals are applied, which helps the comparator to improves its speed, as well as the sampling frequency of the quantizer, 4.4shows the transient analysis of the latched comparator. Here the analoginput signal is compared against last sample signal to see if it is higher then the reference or not. if it is larger then the output is increased else decreased.The density of '1s' and '0s' forming a pulse stream at the output is the digital representation of the input analog signal. A converter needs a sampling frequency more then twice the signal frequency to reproduce the signal without distortion. The density of the pulses represents the average value of the input;

most of the pulses are high for the positive peak of input signal and the density of negative pulses represents the negative peak of the signal.

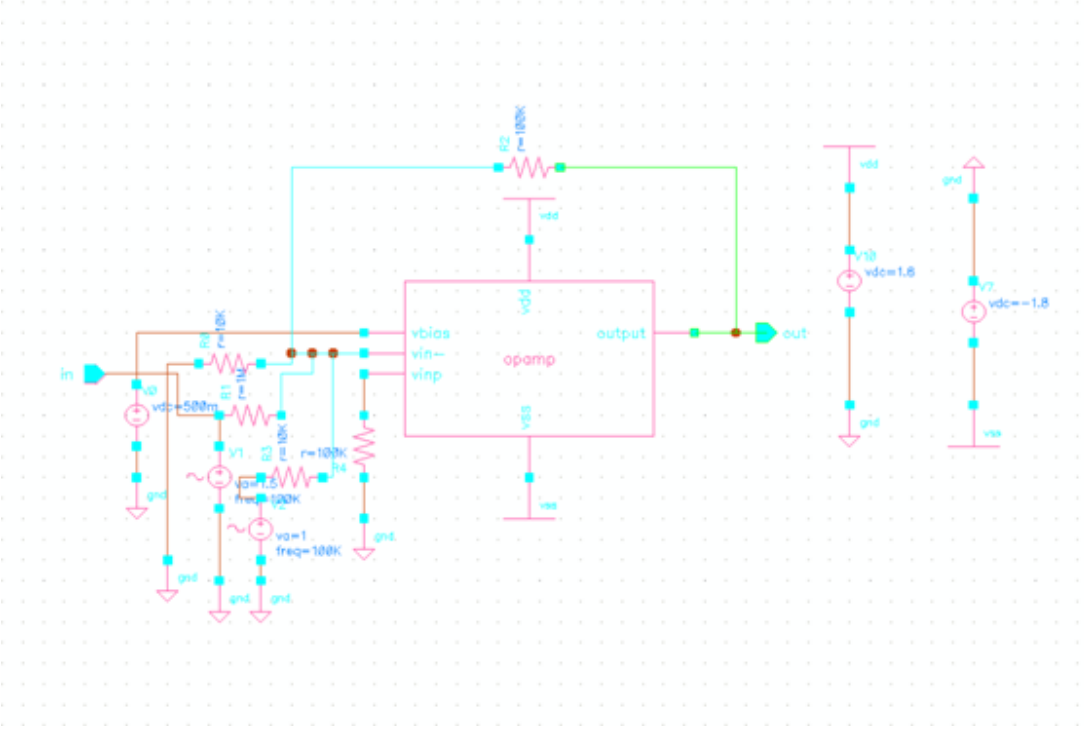


4.4 Simulated waveform of Comparator

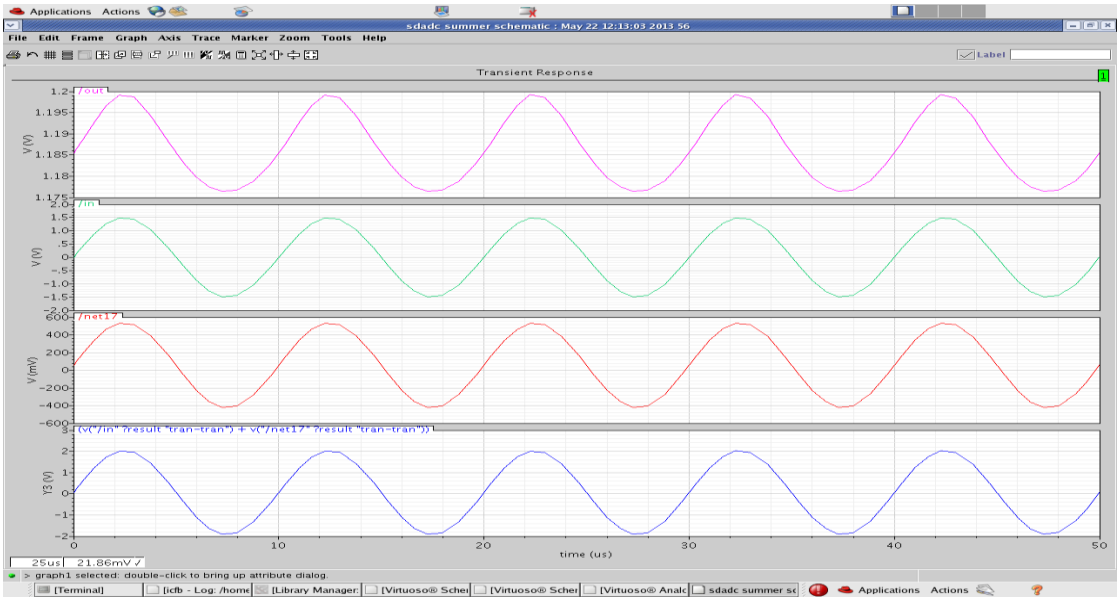
4.4. Designing of Summing Amplifier

The summing amplifier is one of the flexible circuits of Sigma delta ADC. It is given with the analog input signal in one of its terminal and the other is given the feed backed loop from the output of DAC. It is basically a summing amplifier with one resistor in the input side and a combination of resistor for the feedback path also. This circuit is designed using 90um cadence technology. Here a input voltage of 2.5v is given as an input to the summing amplifier and the

corresponding output will be the sum of the input and the feed back voltage 4.5shows the schematic of summing amplifier and 4.6shows the transient analysis of the above circuit.



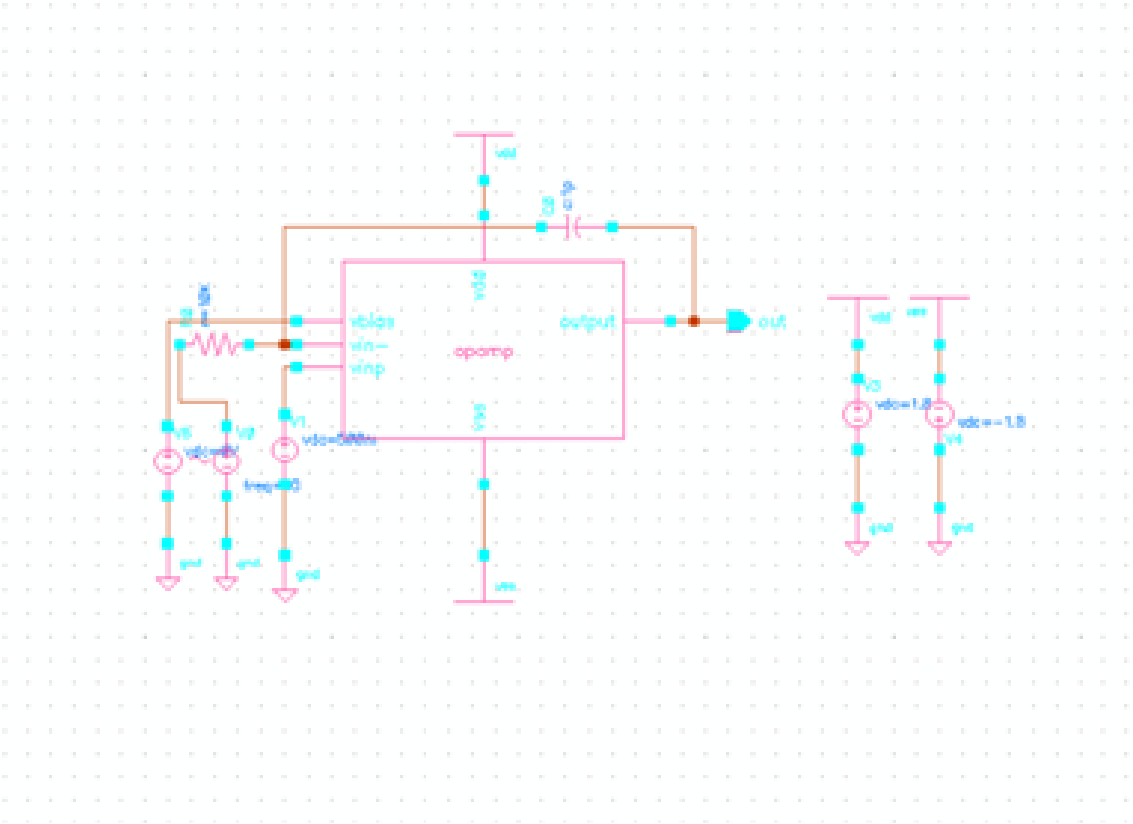
4.5 Schematic of summing amplifier.



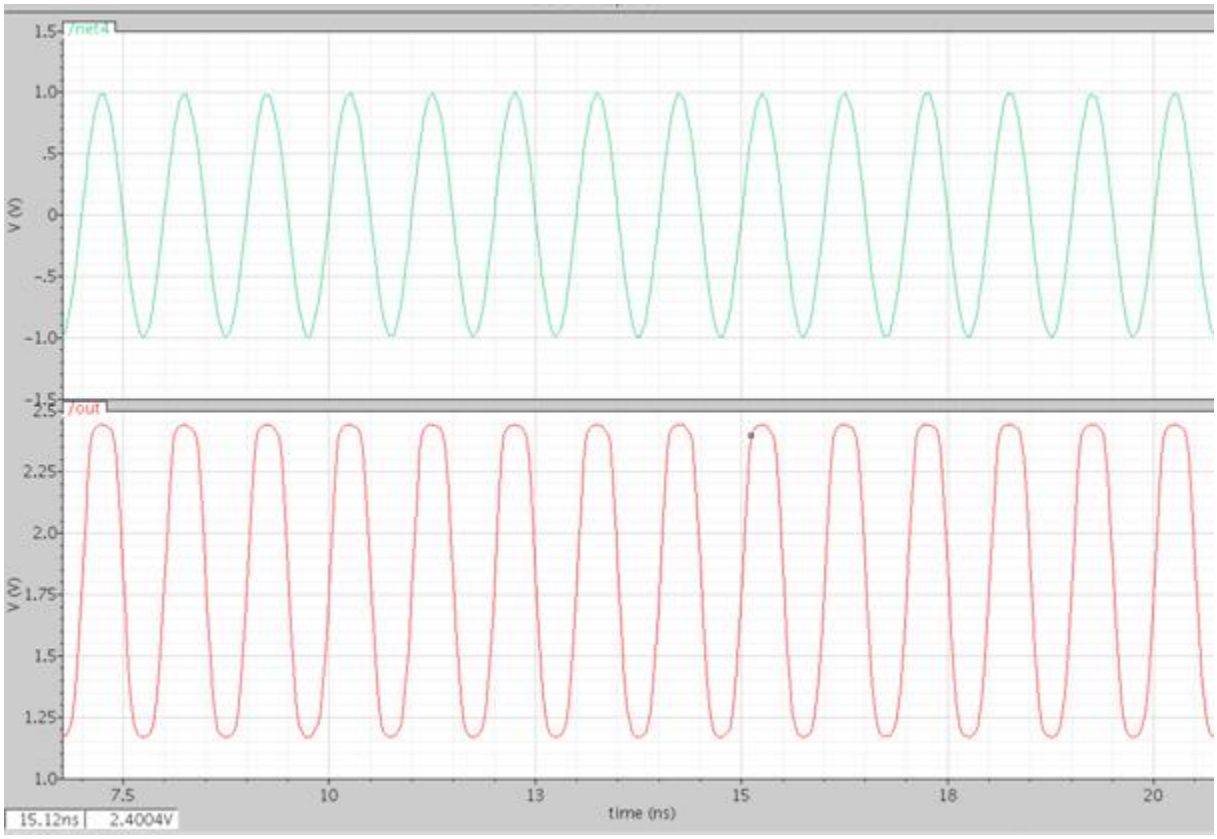
4.6 Simulation result of summing amplifier.

4.5. Designing of Integrator

The integrator is designed using a two stage Op-Amp, in cadence 90um CMOS technology and is connected with a feed back capacitor which helps in charging of the input voltage to give a integrated output. It is given a sinusoidal input signal from the summing amplifier whose output is the sum of the input and the feed back signal and gives ramp output corresponding to a given sinusoidal input. The below 4.7shows the structure of a integrator circuit and 4.8gives the simulation result of the integrator.



4.7 schematic of Integrator

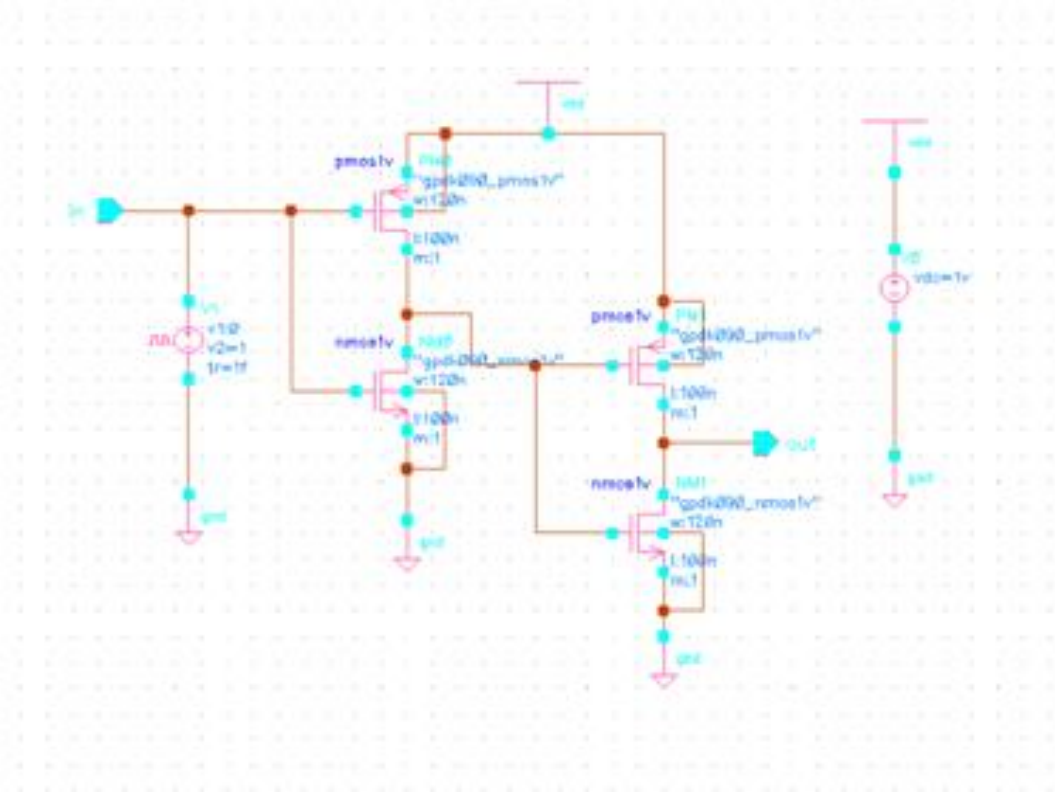


4.8 Simulation Result of integrator

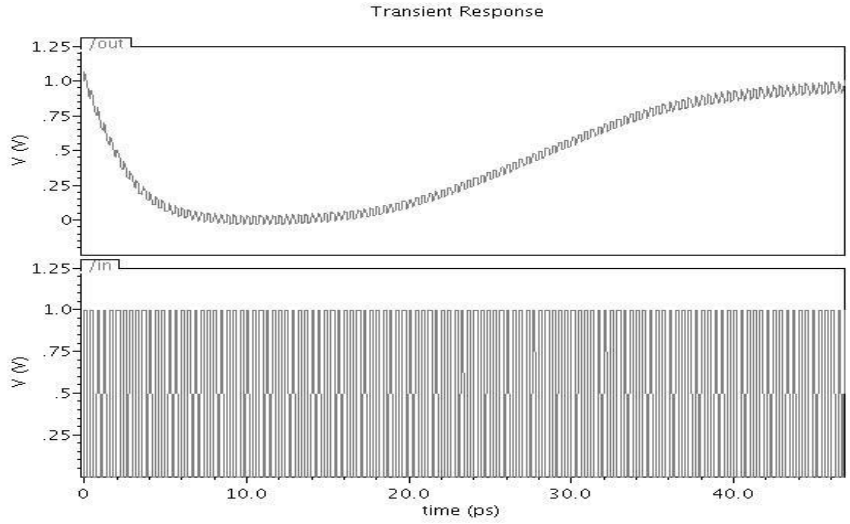
4.6. Designing of Digital-to-Analog Converter

A sigma delta convertor uses multibitquantizerandmultibitdigital-to-analog (DAC) to reconstruct the analog signal,for such DAC the linearity of the convertor is important. For a high resolution DAC, accuracy is one of the major problems that it encounters, for this a single bit system is used to overcome the accuracy problem. In one bit DAC linearity is determined by the accuracy of switching between the reference signal, for high switching accuracy the system will be very linear.4.9shows the basic schematic structure of one bit DAC, the output of one of the invertors

is fed as an input of the other inverter, a pulse input is given to the system and get the corresponding analog output, shown in 4.10



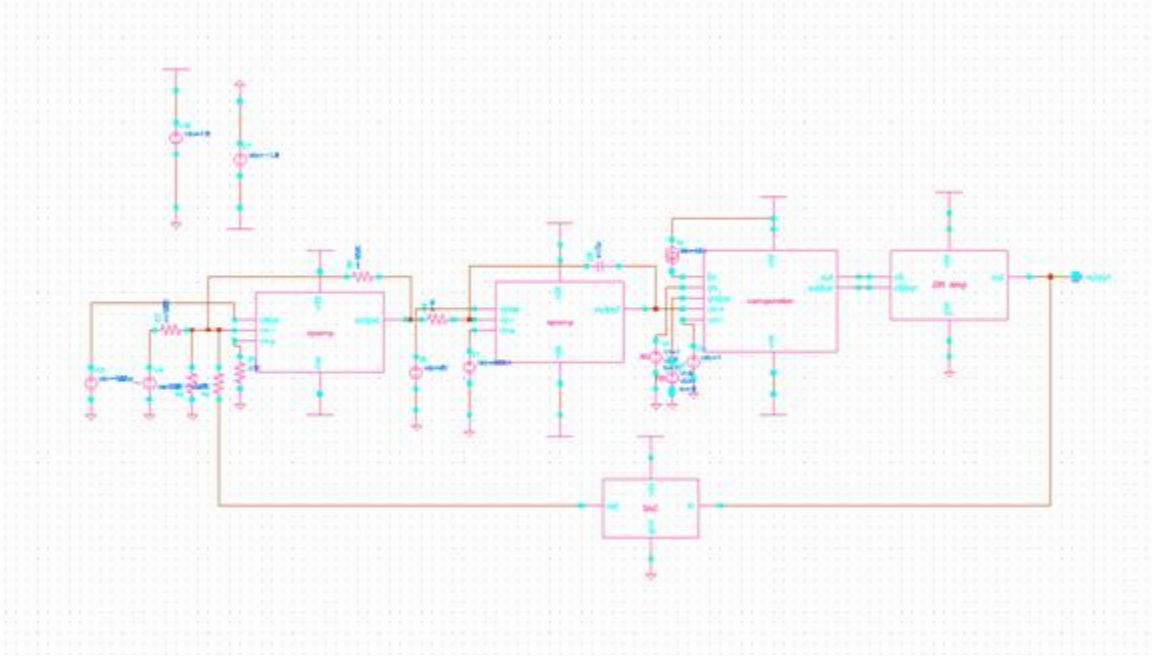
4.9 Schematic of DAC



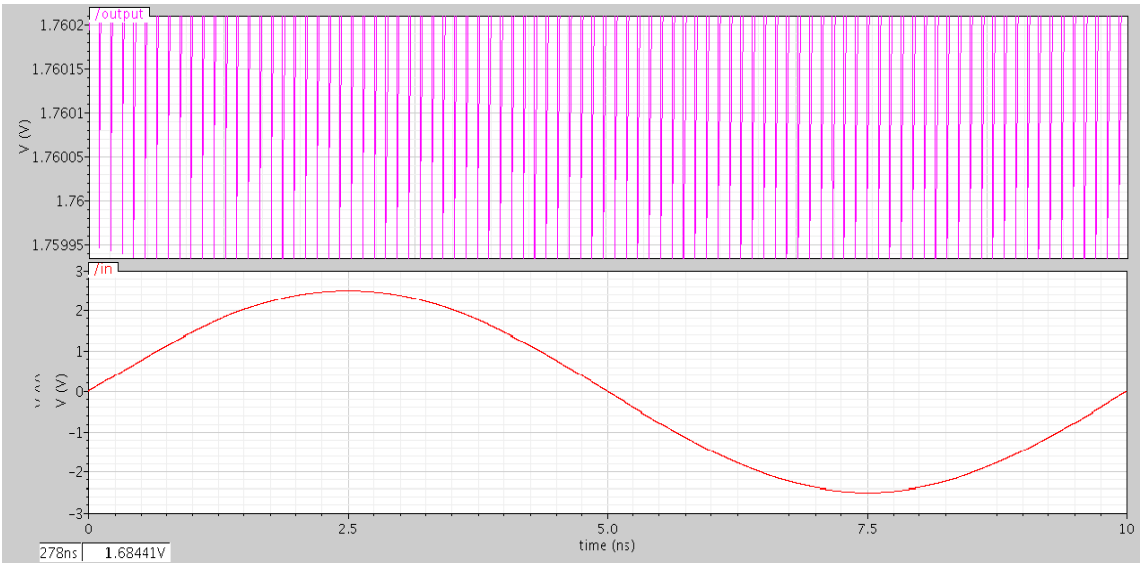
4.10 simulation result of DAC

4.7. Schematic of first Order ΣΔ Modulator:

The sigma-delta A/D converter stands out to be the most advanced, among all the Data converters discussed so far. A block level schematic of a first order A/D converter is as depicted below in Fig4.11.The figure shows the block diagram of a first order Delta-sigma Converter (Σ-Δ ADC). It consists of Integrator, a comparator (1 bit ADC), 1-bit DAC. In above circuitry a 1-bit ADC (generally known as a Comparator), drive it with the output of an integrator, and feed the integrator with an input differenced with the output a 1-bit DAC. The type of A/D converters discussed so far are Nyquist converters where by sampling rate is twice the input signal frequency for error free signal approximation. Only way to decrease the Quantization noise or better signal representation is sampling the signal many more times. This is the fundamental theory in sigma delta data converters.4.11shows the schematic of asigma-delta ADC, the circuit is fed with a sinusoidal signal of 2.5v and frequency of 100MHz to the summing circuit whose other terminal is connected to the feedback output signal of one bit DAC .The output of this circuit is given to the integrator and the other terminal of integrator is connected to a ground. the output of the integrator is given to the latched-comparator, whose other to terminals are connected to clock signals which helps the comparator to increase the speed and also the sensitivity of the circuit. The comparator compares the input signal from the integrator with the reference signal and gives the corresponding output as shown above. It will give a positive signal when ever the input signal crosses the reference signal above its value and a negative when it crosses the reference signal. The pulse of bit generated from the comparator is given as a input to the DAC which is connected as a feedback to the ADSC circuit. This process is iterated several times to get a series of digital bit stream. The simulation result of the above circuit is shown in 4.12below.



4.11 schematic of a sigma-delta ADC



4.12 simulation result of Sigma Delta ADC

The above schematic circuit simulates an input analog signal and there by gives a corresponding digital stream of pulses at the output of the modulator circuits. This is achieved due to the continuous iteration of the input signal to the modulator. At the output of this a decimation filter is used to decimate the oversampled signal and gives a digital output.

5. Conclusion and Future work

5.1. Conclusion

A Sigma delta Analog to digital Convertor is designed by integrating the components of the system.Op-amp which is one of the key components has an open loop gain of 96db and a gain bandwidth of 57 MHz, helps in the smooth operation of the integrator circuit. This is also used as a summing circuit which helps in providing the differential feed back input to the integrator. Followed by a high speed comparator is designed ,for this a latched type comparator is used which compares the input signal with a reference signal and gives the corresponding result which is then fed to 1 bit Digital to Analog (DAC) circuit at the feedback path of the system. This process is iterated and a pulse of digital signal is achieved at the output of the system. The sigma delta ADC was simulated using a standard 0.9μm Cadencetool.Dynamic latch comparator has been designed in order to reduce static power dissipation. The different parts of the dynamic latch comparator like: pre-amplifier, dynamic latch, and output buffer are implemented on CADENCE tool with 1.2 V power supply. The simulation results shown for a sampling frequency of 2.5 GHz and the average power dissipation of the proposed comparator is 68 μW.

5.2. Future Work

The future work of Sigma delta ADC is

1. Design of a high speed high precision reduced size CMOS comparator.
2. Comparison with existing comparator.
3. Designing of a high speed and low power Sigma delta ADC
4. Designing of a multibit Sigma delta ADC.

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